The CDF Silicon Detector Upgrade

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Abstract

A major silicon upgrade project is under way for the CDFII experiment that will operate during Run II of the Tevatron in the year 2000. The innermost detector, SVXII, will cover the interaction region with three barrels of five layers of double sided microstrip detectors. In the radial gap between the SVXII and the new main tracking chamber (COT) will be located the ISL that consists of two planes of double sided miscrostrip detectors at large pseudorapidity and an additional one in the central region. A description of the project design and its motivation is presented here.

1 Introduction

CDFII is the Collider Detector Upgrade at Fermilab scheduled to start operating at the beginning of year 2000. The goal is to accumulate about $3\,\mathrm{fb}^{-1}$ of data at $\sqrt{s} = 2\,\mathrm{TeV}$ with a typical instantaneous luminosity of $2\times10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and a bunch spacing of 396 ns during the first phase and of 132 ns in a second phase. The main guidelines of the silicon upgrade design include: extended geometric coverage of the luminous region increasing the single track acceptance to $|\eta| \leq 2$, 3D track reconstruction capabilities with impact parameter resolution of less than $30\,\mu$m in $r-\Phi$ and less than $60\,\mu$m in z, radiation hardness to cope with the expected delivered luminosity of $\simeq 3\,\mathrm{fb}^{-1}$, digitization and deadtimeless readout in $6\,\mu$s providing data to a Level 2 trigger processor. A fundamental part of the tracking system upgrade is the SVXII[1,2], the innermost vertex detector comprising five concentrical layers of double sided silicon microstrip sensors. Surrounding the SVXII there is the ISL, extending the tracking up to pseudorapidities of $|\eta| = 2$ at a radius of 30 cm. The global tracking strategy will integrate the information from the silicon detectors and

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the main tracking wire chamber (COT), which extends the lever arm for momentum measurements up to 140 cm. A robust tracking system is crucial for a wide range of physics, in particular for new particle searches and heavy flavour physics. For this purpose, a new level 2 trigger (SVT) able to identify secondary vertices using the SVXII information has been designed. CDF has a history of building challenging silicon detectors, the excellent performance of which have been essential to the discovery of the top quark. The size of the new projects is by itself a new challenge given the number of readout channels (from the 46,080 of the predecessors to about 700,000) and the high radiation level to withstand (about 1.5 MRad for the innermost layer).

2 Mechanical Description

The SVXII system is formed by three 29 cm long *barrels* symmetrically located around the nominal center of the detector, covering $2.5\,\sigma$ of the luminous region, see Fig.1. Each barrel contains five concentrical layers of silicon modules,

Fig. 1. View of the three SVXII barrels.

called *ladders*, arranged in a dodecagonal geometry. From the point of view of the readout the fundamental unit is the half–ladder, see Fig.2. It is made

Fig. 2. View of a SVXII ladder.

by a Rohacell foam and carbon fiber rail which supports two silicon sensors microbonded to each other for a total active strip length of 14.9 cm. The full ladder unit is obtained connecting two half ladders together by means of a special carbon fiber bridge leaving the electronics at the two ends. The SVXII ladders are positioned between two intricately machined berillium bulkheads. The bulkheads need to be machined with very tight tolerances since they establish the precision of the alignment. They not only support the ladders but also serve as a heat sink for the electrical components mounted on their ends. The cooling channels are integrated on the bulkheads themselves and a mixture of water and glycol at -5° C in the chiller will be used as a coolant. This will allow to keep the temperature at the bulkhead at about 0° C and the temperature of the sensors below 10° C during nominal operating conditions with an expected power consumption of $\approx 1.8\,$kW for the entire SVXII detector. To avoid gaps along the z coordinate, while keeping the dodecagonal symmetry essential for the SVT trigger, the readout electronics is placed on top of the active sensors. Studies showed that with appropriate shielding this configuration does not introduce a significant additional amount of noise in the system. The readout chips are mounted on a ceramic hybrid constructed using a $500\,\mu$m thick BeO technology which provides good heat dissipation, a high density of connections and the possibility to integrate capacitors and resistors. The gap between the outermost layer of the SVXII at 10.6 cm and the inner screen of the COT at 40 cm is occupied by the Intermediate Silicon Layers (ISL), see Fig.3. The ISL is a mechanically separate device supported

Fig. 3. $r-z$ view of the ISL layers placement. SVXII and COT are also shown.

by a carbon fiber frame that will also serve to support the SVXII. Two ISL layers located at about 20 cm in z from the nominal center provide tracking information in the $1 < |\eta| < 2$ region where the COT efficiency starts degrading. A single central layer (but an additional one is already planned) reinforces the link between the SVXII and the COT. The ISL ladders are made of three silicon sensors bonded togheter supported by a carbon fiber rail for a total length of 22.2 cm corresponding to a input capacitance of less than 30 pF. Due to the large space available at the ISL location the electronic is placed off the sensors, making the hybrid design simpler (thick film on Aluminum Nitrate) and reducing the heat load to the sensors. Moreover, due to the larger radius from the beam, material budget and cooling issues are less crucial.

SVXII parameters	
Number of barrels	3
Number of layers	5
Radius of innermost layer	2.54 cm
Radius of outermost layer	10.6 cm
1/2 ladder length	14.5 cm
n-side readout angle ($^\circ$)	$90, 90, 1.2, 90, -1.2$
Readout pitch p-side (μm)	$60, 62, 60, 60, 65$
Readout pitch n-side (μm)	$141, 126, 60, 141, 65$
Readout channels p-side	211,968
Readout channels n-side	193,536
ISL parameters	
Number of layers	3
Radius of layers (cm)	20,22,28
1/2 ladder length	22.2 cm
Readout coordinate	$\Phi + \Phi'(1.2^\circ)$
Readout pitch p,n-side (μm)	112, 112
Readout chips total	2400
Readout channels total	307,200

3 The Silicon Sensors

The SVXII sensors are all double sided providing $r - \Phi$ and z coordinate measurement, the latter using a combination of 90° (for layers 0, 1 and 3) and small angle stereo $\pm 1.2^\circ$ (layers 2 and 4) strips. The 90° points allow a precise measurement of the z coordinate of the primary interaction vertex while the small angle stereo will greatly help the pattern recognition. A substantial R&D program on silicon sensors has been carried out to achieve the full potential of this tracker upgrade[3]. This has resulted in significant developments in the areas of capacitance and microdischarge minimization, geometrical layout optimization, availability of large area detectors from 6" Si wafers and determination of processing and operating conditions. The 90° sensors are made by Hamamatsu Photonics with a double metal technology. To optimize the strip isolation on the n side while minimizing the interstrip capacitance, a combination of individual and common p-stops has been used. Moreover, since these detectors will be the closest to the interaction point with an expected dose of about 0.5 MRad/fb^{-1} at layer 0, they will be operated with split bias voltage to account for the overdepletion voltage needed after type inversion, while minimizing microdischarge possibility. In Fig.4 are shown the results from a Test Beam of Hamamatsu prototype sensors unirradiated and irradiated up to a dose of 1.3 MRad (with 8 GeV protons). Even after irradiation, by increasing the bias voltage, it is possible to recover good performances and collect the full signal with a degradation in S/N of only 10%. The small an-

Fig. 4. S/N for Hamamatsu SVXII sensors before and after irradiation as a function of V_{bias}

gle stereo detectors are manufactured by Micron Semiconductors using 6" Si wafers. The large available area allows to place two sensors on a single wafer (SVXII layer 2 and layer 4) thus reducing processing costs. A layer 2 prototype from Micron has been studied at a Test Beam and its performances are very good (see Fig.5): the signal is fully collected on both sides at about 20 V overdepletion and the S/N is above 25 as expected for a single sensor. The Test Beam data were taken at 25 MHz while running condition will be at 53 MHz. The estimated degradation of the noise figure is approximately a factor 1.4 for the latter configuration. For the ISL detector there is only one sensor

Fig. 5. Signal for Micron SVXII L2 sensor as a function of V_{bias}

design, also double sided, with small angle stereo readout on the n-side, such that two ISL sensors fit on a single 6" wafer.

4 Frontend Electronics

The SVXII frontend electronics consists of a radiation hard CMOS custom integrated circuit (SVX3 chip [4,5]) optimized for 396 ns and 132 ns bunch crossing interval. Chips are controlled over a high density copper cable trough auxiliary cards positioned just outside the outermost SVXII layer, one for each wedge. The chip, with 128 parallel input channels, is capable of performing simultaneous analog and digital operation. The Front End section contains the input amplifier and integrator (107 ns shaping time), the pipeline and the logic necessary to control the pipeline and buffer control functions. The pipeline depth of 42 cells is set by the Level 1 trigger maximum latency of 5.5 μs at 132 ns. By having also four extra cells to hold data for later processing, and by being able to write analog data into pipeline cells while bypassed cells are being digitized and readout, the SVX3 chip is capable of operating with negligible deadtime for Level 1 trigger rates up to 50 kHz. The Back End section performs the operations of digitization (7 bit) and sparsification, that is only a channel over a pre-set threshold and its two closest neighbours are read out. The highly parallel fiber readout system that follows the wedge geometry feeds the SVXII $r - \Phi$ information to the Level 2 SVT trigger in about 6 μs and completes the full readout in about 10 μs. Two of the most critical specifications for the chip are the noise level and the radiation hardness. The noise performances have been studied on different versions of the chip. The prototypes have been fabricated in radiation soft version by Hewlett Packard and radiation hard by Honeywell: no difference in performances is seen between the rad-soft and rad-hard version. The noise should vary between 1200 and 2000 electrons depending on the C_{in} and the mode of operation. The preproduction chip, SVX3d, has been submitted and the rad-hard version should be ready for June.

5 Conclusions

The CDFII silicon upgrade, comprehensive of the SVXII and ISL detectors, is expected to become operational in year 2000. This is an ambitious project both for the number of channels and for the hostile radiation environment of Run 2. An extensive program of research and development of double sided silicon sensors carried out in close contacts with the manufacturers has resulted in optimization of the design and processing steps of the production sensors (double metal technology, 6" wafer). The results from the latest Test Beam using prototype sensors from Hamamatsu and Micron at 25 MHz are very good and consistent with expectations. The preproduction version of the readout chip has been submitted and the experience gained with the previous versions lead us to believe this has good chances to be the final one.

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