Technical Information Manual

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MOD. V 789

32 CH. ICARUS
DIGITAL BOARD

NPO:
00100/98:V789x.MUTx/01

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. GENERAL DESCRIPTION

1.1 Overview

The CAEN Model V789 ICARUS digital board is a 32-channel digitizer readout board specially designed for the ICARUS experiment [1]. This board is the evolution of a prototype (ARIANNA board) described in [2]. This board is housed in a 1-unit wide VME module and its function is to read the digital data coming from the Model V791 (ICARUS analog board) and to store them in a Multi Event Buffer (MEB) memory, according to a complex, programmable trigger logic.
The digital data are transferred to the module via a fast link (21-bit word, 40 MHz frequency). Each word contains two ADC-data (10 bit + 10 bit) and a SYNC signal (1 bit). The two ADC-data refer to two 16-channel groups that have been multiplexed temporally, whereas the SYNC signal tags the channel 0 of each 16-channel group. In the whole, the module takes 400 ns to read out the 32 channels.
In order to allow the test of the module also without the link, some test patterns are stored in a relevant FIFO memory. These test patterns, thus, can substitute the input data from the external ADCs.
Each 16-channel group can be seen as an independent unit: only the absolute time counter, the test pattern FIFO memory and the VME interface are common to both the groups.

The digital data are stored in a static RAM divided into a programmable number of Circular Buffers. The write access to the buffers is controlled by the trigger logic, which is sensitive to the PEAK signals generated by two DAEDALUS chips [1,2], one for each 16-channel group. In particular, each DAEDALUS chip can be seen as constituted by four independent units, each of which controls 4 channels. The detection of a PEAK on one of the channels causes the following:
1) the data in the presently pointed buffer are frozen,
2) the buffer is enabled to be read out via VME,
3) a set of external triggers are generated.

If other buffers are ready to be written on, the data acquisition continues in the following buffer. This operation can occur also as a consequence of specific external triggers. A parallel task provides to store useful information concerning the event (absolute time tag, trigger specifications, etc.) in the Header FIFO.
The RAM memory which contains the samples of the stored waveform can be accessed via VME, as well as the FIFO memory. Both the buffer and trigger controls are programmable via VME.
Each DAEDALUS chip is located on a piggy-back board in order to allow possible test procedures independently from the V789 module.

1.2 Functional block diagram

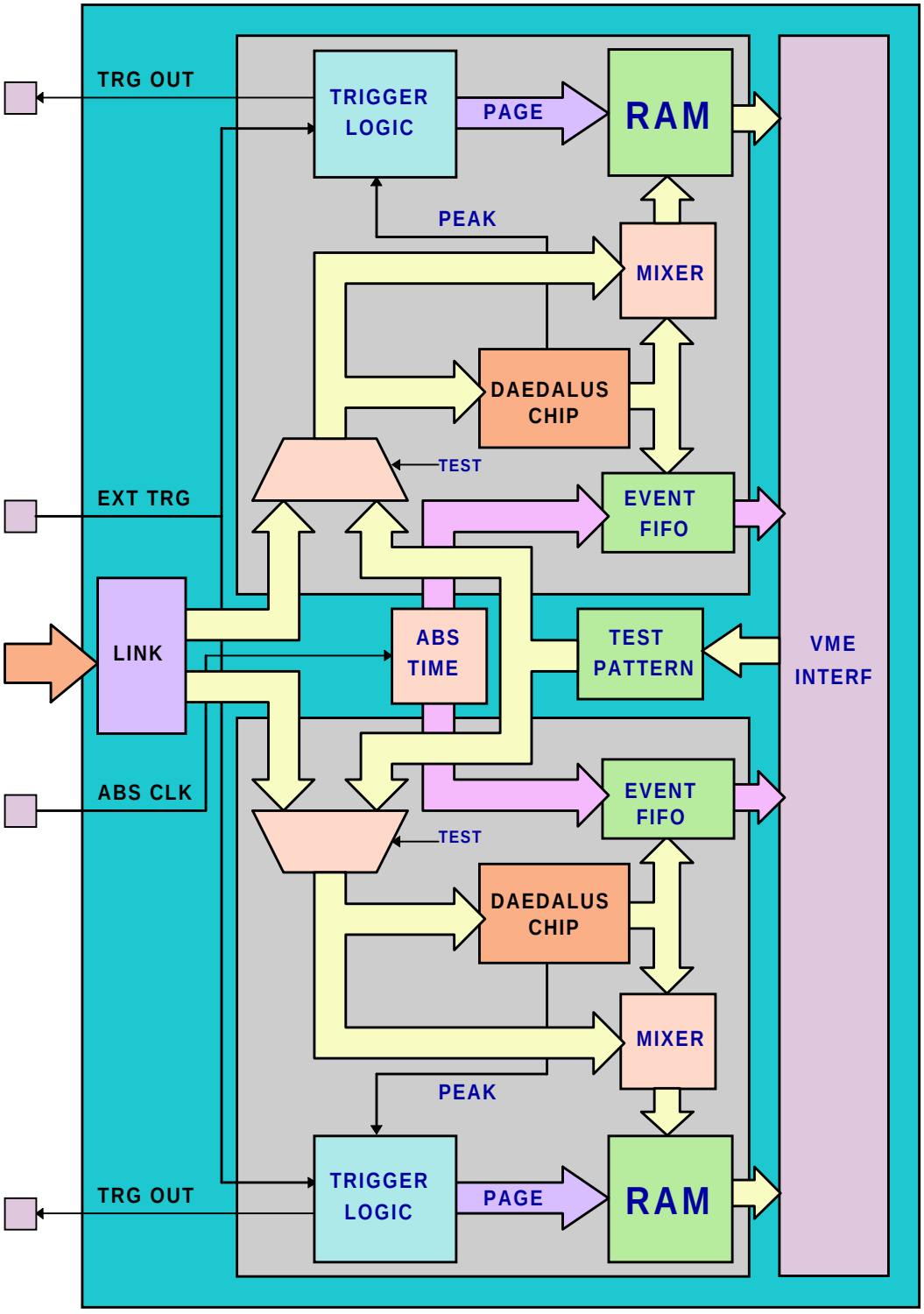


Fig. 1.1 - Functional block diagram of the V789 module

1.3 Main Technical Specifications

Package:	1-unit wide, 6-unit VME Module; P1 and P2 connectors (PAUX connector is optional).
Number of channels:	32 channels divided into two independent blocks (block A = ch[15:0], block B = ch[31:16];
Input samples:	10 bit double data, 40 MHz (16+16 channels multiplexed in time);
Sample Rate:	2.5 MHz
Absolute time:	32 bit counter at 25 MHz (in the whole about 172 sec)
Trigger sources:	Peak detection, Left/Right Trigger, GLOBAL Trigger, EXT Trigger, VME Trigger
Memory:	Multi Event Buffer. 8Kword per channel, to be divided into buffers with programmable dimensions from 64 to 4096 words.
Test Pattern:	10 bit, 1Kword (common to all the 32 channels)
VME:	Registers: Single Access, A32, D16 mode. Output Buffer: Single Access or BLT access in A32, D32 mode. Interrupter with fixed priority.

2. TECHNICAL SPECIFICATIONS

1.1. Packaging

The V789 module is a 1-unit wide, 6-unit high VME board using the P1 and P2 connectors (PAUX connector is optional). It is made up by a motherboard and two piggy-back boards containing one DAEDALUS chip each.

2.1 Power requirements

The board has only one power supply source of 5 V with an absorption of 1 A.
All the board components, in fact, work with 3.3 V: thus, there is a local regulator to transform the board power supply from 5 V to 3.3 V. The regulator is available in two different versions: the first is a linear regulator using a Low Drop regulator with an external MOS; the second version is a switch-type regulator implemented with a integrated controller and two external MOS devices. The User can choose which regulator version has to be mounted at the factory.

2.2 External connections

2.2.1 Connectors

1 3M 10214-5215JL Mini D-Ribbon female Connector for the connection to the V791 analog module.
1 SMB Radiall R114 665000 Connector for LEFT TRIGGER IN
1 SMB Radiall R114 665000 Connector for RIGHT TRIGGER IN
1 SMB Radiall R114 665000 Connector for GLOBAL TRIGGER IN
1 SMB Radiall R114 665000 Connector for LEFT TRIGGER OUT
1 SMB Radiall R114 665000 Connector for RIGHT TRIGGER OUT
1 SMB Radiall R114 665000 Connector for GLOBAL TRIGGER OUT

2.2.2 Front panel LEDs

1 "DTACK", green LED: read/write access to the board via VME;
1 "FULL", red LED: at least one of the two MEB is full;
1 "DRDY", yellow LED: at least one of the two MEB contains data;
1 "TRIG", green LED: trigger accepted by one of the two blocks A and B;
1 "OVFL", red LED: at least one of the two DAEDALUS chips is in Overflow.

2.2.3 Signal characteristics

Table 2.1 - Main features of the signals

Name	D	Connector	Level	Logic	Notes
ABS_CLK	I	CK lines of the PAUX or P2 (differential)	TTL	Rising Edge	Clock of the absolute time counter (25 MHz)
ABS_RES	I	CL lines of the PAUX or P2 (differential)	Differential TTL	Active	Reset for the absolute time counter
EXT_TRG	I	SG line of the PAUX or P2 (half line diff.)	Single ended TTL	Active	External Trigger
TRG_EN	I	SG line of the PAUX or P2 (half line diff.)	Single ended TTL	Active	Enable for the triggers generated by the PEAK and for the LR-TRIG.
LT_IN	I	SMB on the panel	Single ended TTL (term. with 50 Ω)	Active	Left Trigger input (from the adjacent module)
LT_OUT	O	SMB on the panel	Single ended TTL	Active	Left Trigger output (to the adjacent module)
RT_IN	I	SMB on the panel	Single ended TTL (term. with 50 Ω)	Active	Right Trigger input (from the adjacent module)
RT_OUT	O	SMB on the panel	Single ended TTL	Active	Right Trigger output (to the adjacent module)
GT_IN	I	SMB on the panel	Single ended TTL (term. with 50 Ω)	Active	Global Trigger input
GT_OUT	I	SMB on the panel	Single ended TTL	Active	Global Trigger output
LINK	I	Mini Delta Ribbon	Four LVDS lines	-	Link to the V791 analog module.

N.B. Differential TTL and single ended TTL are meant with a 3.3 V voltage level.

Bit 20	Bits 19...10	Bits 9...0
1	CHANNEL 16	CHANNEL 0
0	CHANNEL 17	CHANNEL 1
0	CHANNEL 18	CHANNEL 2
0	CHANNEL 19	CHANNEL 3
0	CHANNEL 20	CHANNEL 4
0	CHANNEL 21	CHANNEL 5
0	CHANNEL 22	CHANNEL 6
0	CHANNEL 23	CHANNEL 7
0	CHANNEL 24	CHANNEL 8
0	CHANNEL 25	CHANNEL 9
0	CHANNEL 26	CHANNEL 10
0	CHANNEL 27	CHANNEL 11
0	CHANNEL 28	CHANNEL 12
0	CHANNEL 29	CHANNEL 13
0	CHANNEL 30	CHANNEL 14
0	CHANNEL 31	CHANNEL 15

Fig. 2.1 - The 21-bit output data packet of the link

The 21-bit output of the link is composed as follows (please refer to Fig. 2.1):
10 bits referring to block A (channels from 0 to 15);
10 bits referring to block B (channels from 16 to 31);
1 bit referring to the SYNC signal (active) which marks the channel 0.

The ABS_CLK, ABS_RES, EXT_TRG and TRG_EN signals are sent to all modules contained in a single crate via the differential CK, CL and SG lines of the VME JAUX or via the user-defined lines of the J2 (A873 backplane required). These lines are terminated on the backplane directly or on the A873 board.

N.B.: the use of the J2 bus for the transmission of these signals requires the installation of the A873 ICARUS connecting board.

The distribution of these signals can be extended to all crates via a fan-out with NIM outputs (refer to Fig. 2.3). The signals coming from the fan-out are then received locally in each single crate by a relevant board (Model V816, digital service board). This board provides to turn them into TTL signals and to transmit the latter via the JAUX or J2 bus.
The ABS_CLK signal has a typical frequency of 25 MHz.
The TRG_EN signal allows to generate an 'acquisition window' within which the trigger signals are accepted. The module does not accept any trigger signal which occurs outside this acquisition window, except for the VME trigger, the external trigger and the Global trigger.
The Left and Right Trigger signals allow to propagate the trigger signal generated by a 16-channel group to the adjacent groups in order to get more information about the PEAK which has caused the generation of the trigger itself. The two A and B channel blocks inside a single V789 module are already connected to each other through internal Left/Right Trigger lines, as shown in Fig. 2.2:

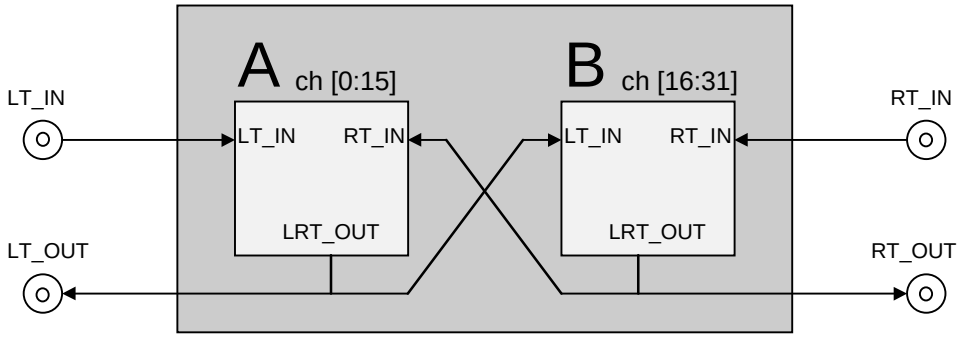


Fig. 2.2 - The two channel blocks A and B and their connection inside a V789 module

The following figure shows a typical connection of the V789 modules inside the VME crates.

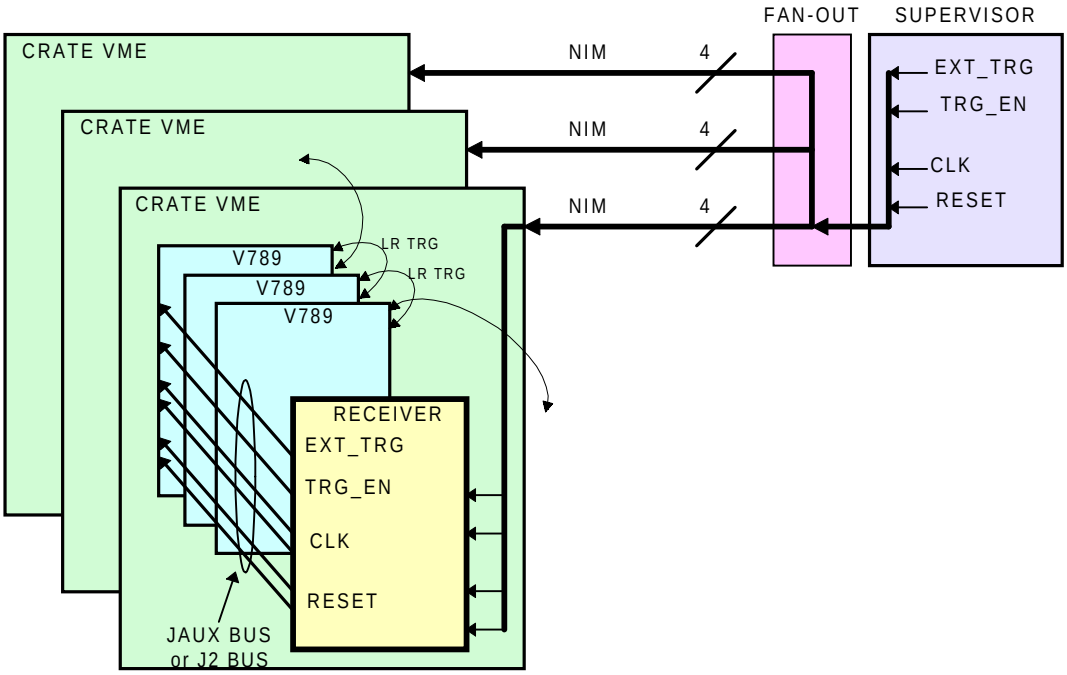


Fig. 2.3 - Connection of the V789 modules inside a VME crate

2.2.4 Internal hardware settings

The default hardware-cabled interrupt line is on the IRQ3 line of the VME. It is anyway possible to change it with any of the other seven IRQ lines of the VME interface by cutting the default soldering and then joining the preferred IRQ line with solder.

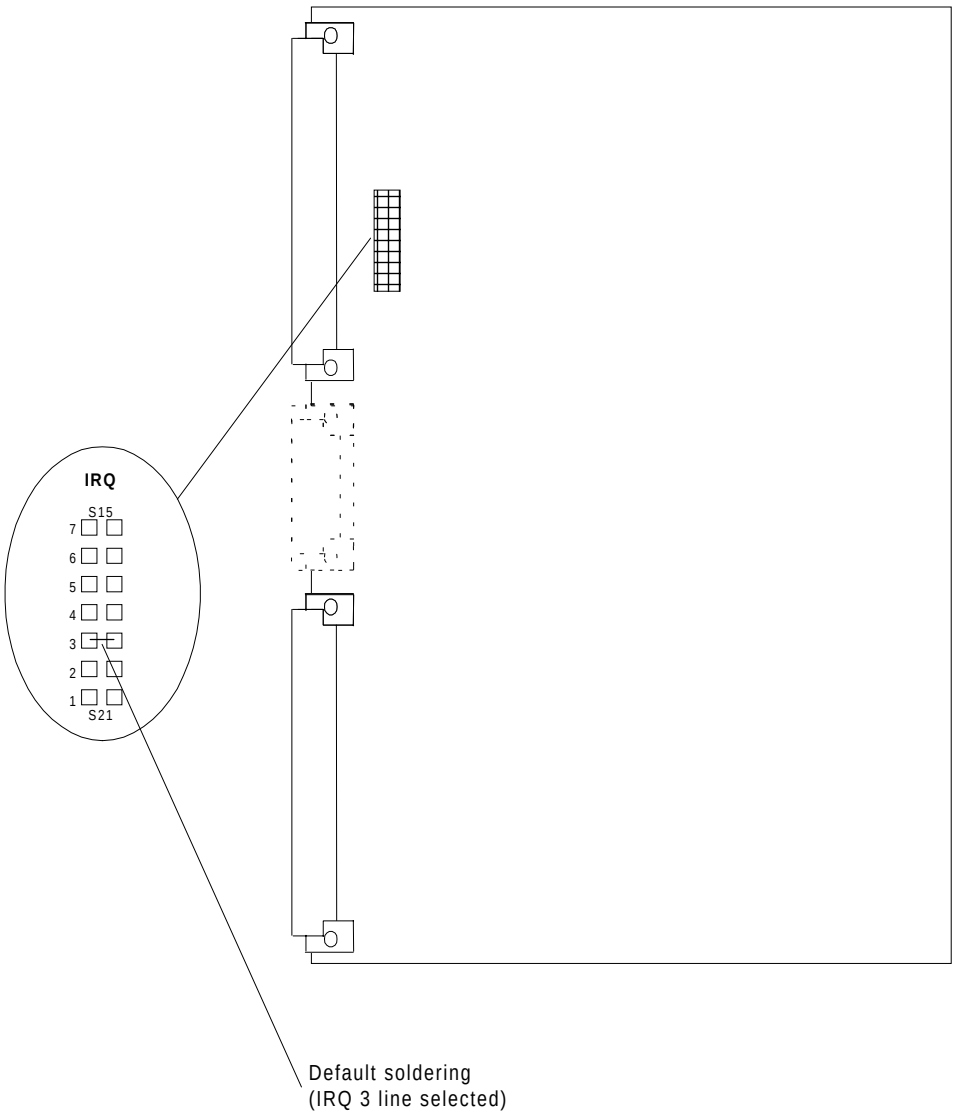


Fig. 2.4 - Soldering face of the V789 module

3. HARDWARE DESCRIPTION

3.1 Detailed block diagram

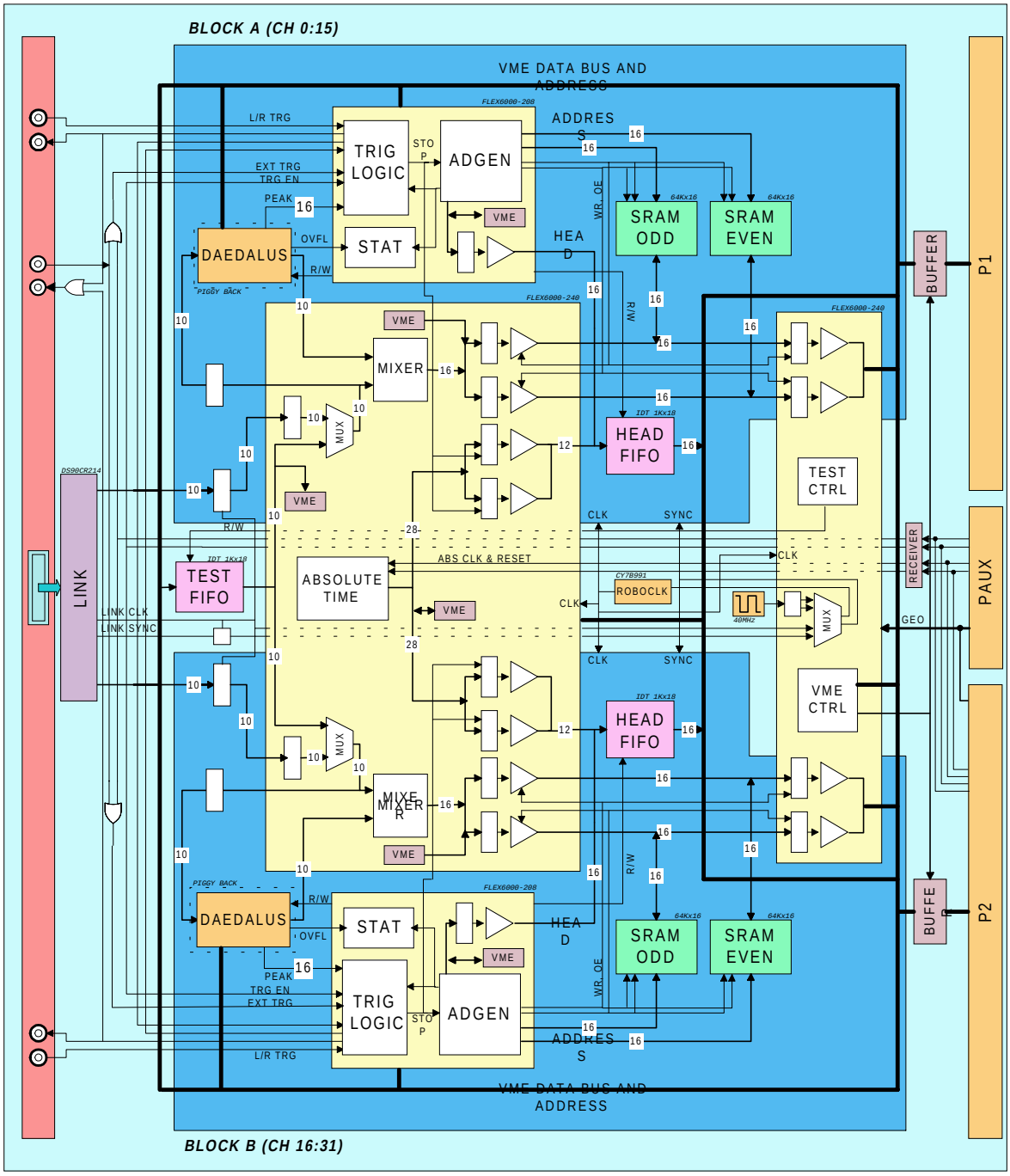


Fig. 3.1 - Detailed block diagram of the V789 module

3.2 Data flow

During normal operation the data (one 10-bit word for each channel block) come from the link at a frequency of 40 MHz and are resynchronised by a latch directly via the clock signal coming from the link itself. This allows to make steady the data for almost a whole period. The data are then synchronised with the board global clock inside the PLD V789MIX. They are then transferred from the PLD to the DAEDALUS chip and sent again to the PLD and mixed with the data coming from the link. The final result is a 16-bit word to be written in the SRAM.
The SRAM read/write accesses are controlled by the ADGEN block placed inside the PLD V789CTRL. There are two 16-bit buses which are used to transfer the data from the mixer to the SRAM and from the SRAM to the VME interface, alternatively. This functional principle is summarised in the following figure:

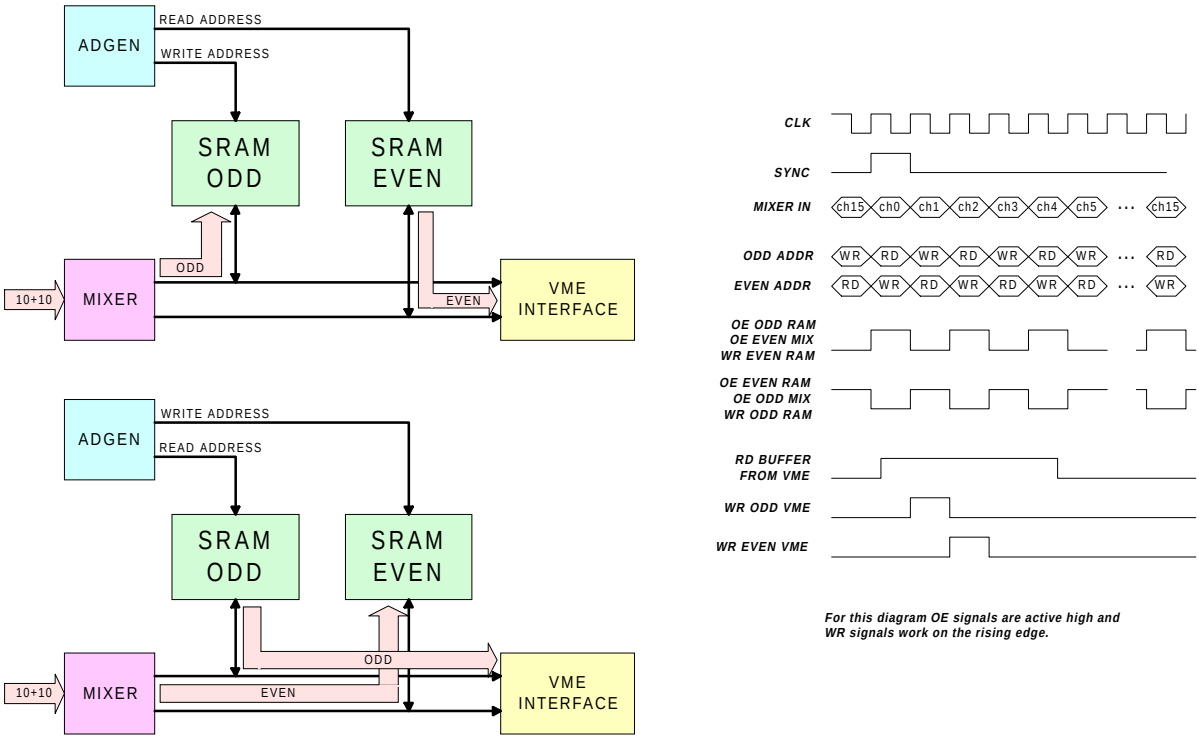


Fig. 3.2 - Functional principles of the SRAM read/write accesses in the V789 module

The datum sent to the VME interface is strobed in a register of the same interface by the ADGEN block as soon as a MEB read access is serviced. This operation involves both the ODD and the EVEN data, according to the relevant timing. In this way a 32-bit datum, ready to be transferred on the data bus, is available at the VME interface. In fact, the MEB is seen from the VME as it were a FIFO.

3.3 Multi Event Buffer

The RAM memory of the V789 module is organised according to the typical MEB logic. In the whole there are 8 K available for each channel and these can be divided into a set of buffers the dimensions of which are programmable by the User according to the following table:

Table 3.1 - Programming of the buffer dimensions

MODE	N. samples per buff., per ch.	N buffer	read/write pointer nr. bit
0	64	128	7
1	128	64	6
2	256	32	5
3	512	16	4
4	1024	8	3
5	2048	4	2
6	4096	2	1
7 (test mode)	8	2	1

The converted data are written continuously (40 MHz) in the active write buffer, i.e. the buffer pointed by the write pointer. This buffer acts as a circular buffer. On the other hand, it is possible to read via VME the buffer pointed by the read pointer. The read operations are independent from the write operations.
The write pointer is automatically incremented as soon as a trigger occurs, while the read pointer must be incremented via software by means of a write access to the INCBP register. The sample readout inside a buffer is performed sequentially starting from the first sample. As soon as the end of the buffer is reached, if the read pointer is not incremented, the readout starts again from the first sample in the same buffer. The MEB is read via VME in D32 mode. Each long-word contains the data relative to two adjacent channels (0 and 1, 2 and 3, ... 14 and 15). Each sample (2.5 MHz) occupies 8 long-words of the buffer.
Please note that in the memory buffer the '*first datum*', in a temporal sense, is NOT the datum which physically occupies the first location. This does not mean that the first datum for the buffer is the first datum (in a temporal sense) written as a consequence of a trigger signal. The actual temporal sequence of the data must be reconstructed via software by starting from the stop address that is read in the header of the event.
In particular, the stop address tags the datum relative to the channels 0 and 1 of the last sample memorised in the buffer: thus, the first datum, in temporal order, is placed in the following location of the buffer:

First_sample(ch 0, ch 1) = ((STOP_ADDR * 8) + 8) mod (Nbuf * 8).

The following figure is an example showing how the sample sequence can be shifted with respect to the actual temporal sequence:

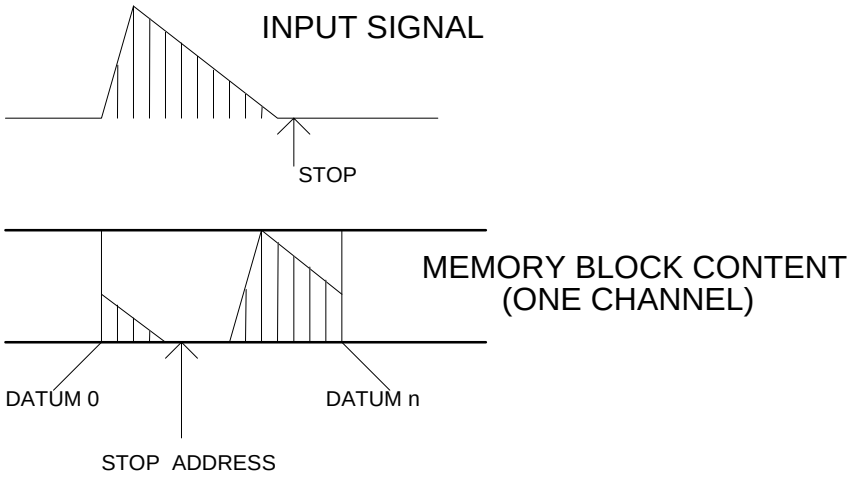


Fig. 3.3 - Sample sequence and temporal sequence in the buffer

The MEB can be in three different conditions: *Full*, *Empty* or *Not Empty*. The status of the MEB can be read in the STAT register (refer to Section 4.4.14) relative to each 16 channel block. Via VME it is possible to read the positions of the read and write pointers.
If these are different, the MEB is in the *Not Empty* status.
If they are equal, the MEB can be either *Full* or *Empty*, depending on the last operation performed on the pointers.

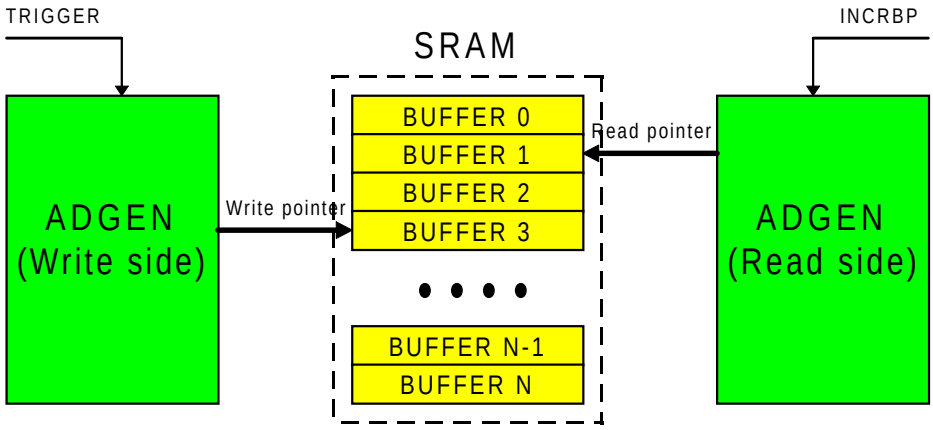


Fig. 3.4 - Read and Write access to the MEB of the V789 module

3.4 The DAEDALUS chip

The new DAEDALUS chip is constituted by 4 independent units, equal to each other, each of which elaborates the data relative to 4 channels. This is the reason for which the Chip Select (CS) command is not common to the whole chip but the User must generate 4 CS commands with the relevant timing. The data for the register programming as well must be regarded as divided into 4 parts of 4 bits each (refer to the Figure below).

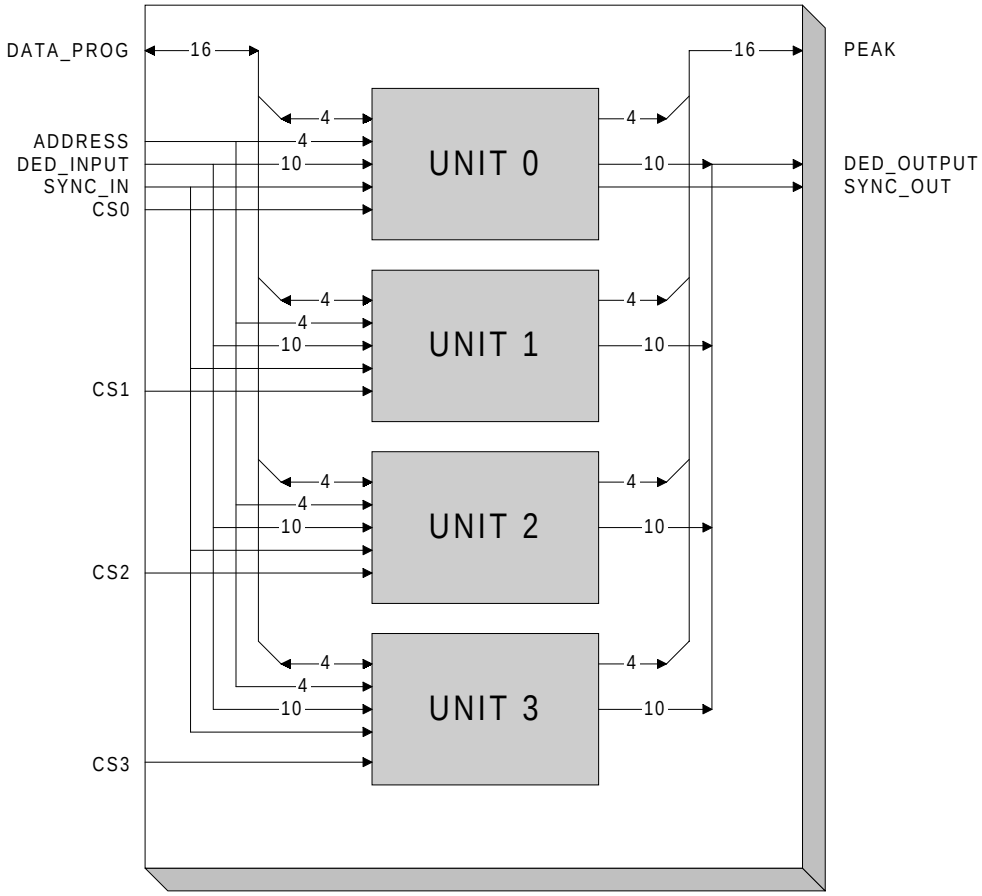


Fig. 3.5 - The DAEDALUS chip: block diagram

This chip receives the 10-bit input data relative to 16 channels multiplexed in time. The input data frequency is 40 MHz (which corresponds to a sampling rate of 2.5 MHz on the signal). The data are elaborated in order to detect the presence of peaks in the various channels. The detection of a peak causes the setting of the lines called PEAK. Moreover, the filtered data, multiplexed according to the same criterion adopted for the input data, are available as well at the output of the chip. The SYNCI signal tags the channel 15 at the DAEDALUS input and the SYNCO signal tags the channel 0 at the output.
The following figure shows the timing of both the input and output signals, while the table below lists all the input and output signals.

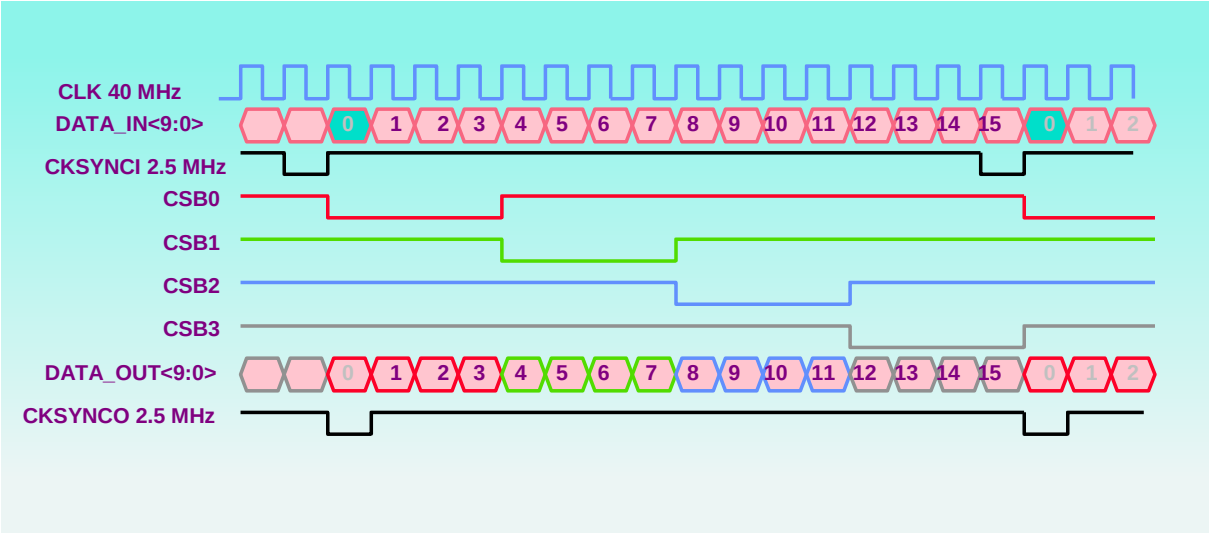


Fig. 3.6 - Timing of the input and output signals

Table 3.2 - List of the input and output signals of the V789 module

Name	Type	Signal
PEAK<15:0>	output	16 bits (one for each channel) that flags an peakfound
ADDRESS<3:0>	input	4 address for parameters registers address
PROGDATA<15:0>	i/o	Data bus for parameters read/write
OFL	output	Overflow: it goes 1 when an overflow occurred in the chip
DED_OUT<9:0>	output	10 bit DAEDALUS data output
DED_IN<9:0>	input	10 bit DAEDALUS data input
CSB<3:0>	input	Chip select: active low. It enables the I/O function of the correspondent 4 channel group. When data outputs are in HZ and data inputs are disabled
STROBE	input	Used to latch on rising edge the parameters into the registers
CKSYNCO	output	Active low: the PEAK outputs must be sampled when this signals is active
RESDED	input	Active low. It acts on the control logic. The median filter and parameters registers are not cleared by this signal
OEDED	input	It enables the read/write operation of the registers. =0: WRITE =1: READ if =1 the chips drives the PRGDT<15:0> lines
CKSYNCI	input	Active low it synchronise the chip with the external logic. It indicates when the channel0 data is sampled.
CKDED	input	CLK 40 MHz
TEST	input	Test Pin. In normal operation mode it must be low.

3.5 Trigger Logic

The trigger logic accepts the following input trigger sources:

- PEAK <15...0> these signals come from the DAEDALUS chip;
- TRIGGER LEFT it comes from an adjacent board;
- TRIGGER RIGHT it comes from an adjacent board;
- EXTERNAL TRIGGER this is an external trigger;
- GLOBAL TRIGGER It is equivalent to the external trigger;
- VME TRIGGER it is a software trigger used for testing purposes.

The first three types of trigger signals (PEAK <15..0>, TRIGGER LEFT, TRIGGER RIGHT) are generated due to the detection of a peak on the channels and hence are also called HIT FOUND trigger signals. All these triggers are maskable via VME.
Another signal which plays an important role in the trigger logic is the TRG_EN signal, which is an external signal coming from the PAUX or P2 connector. The TRG_EN signal allows to generate an '*acquisition window*': if the Trigger signals (except for the VME, the external and the global triggers) occur outside this acquisition window, they do not cause the storage of the buffer in the memory. Please note that the TRG_EN signal is not an inhibit signal of the trigger: actually, even if the TRG_EN is not active, the occurrence of a trigger enables the control logic which counts the number of samples to be saved in the buffer. As soon as the present buffer is ready to be frozen, if TRG_EN is active, the actual storage of the buffer occurs and the pointer goes to a new buffer; otherwise, the same buffer keeps on being written and the old samples will be overwritten (in this case it is as if the trigger had never arrived).
In the following we will indicate a trigger as signal which causes the storage of an event.
The data must be memorised in the buffer as follows (refer to Fig. 3.7):

- **Nbuf** number of total samples for each channel,
- **Npre** number of samples before the occurrence of the trigger,
- **Npost** number of samples after the trigger.

The meaning of these parameters is also shown in Fig. 3.7, where the relevant windows are also indicated together with a HIT FOUND trigger signal. As far as new or still active triggers are concerned, the hit window acts as an 'inhibit window', while the post-hit window as an 'active' one: this is because during the hit window no other trigger signals are accepted whereas during the post-hit window a new trigger or a possible still active trigger (a VME, external or global one) is accepted.
Nbuf is programmable in 7 steps (64, 128, 256, 512, 1024, 2048, 4096).
Npre and *Npost* are completely programmable: it is up to the User to set these values coherently.
After the occurrence of a trigger, the trigger logic verifies that there are at least *Npre* samples already memorised; if there are, it goes on memorising other samples as long as the required total number of samples to be memorised (*Nbuf*) is reached. Then it freezes the buffer and goes to the following one. This operation is performed by taking also into account the DAEDALUS latency time. In the case that there are not all the *Npre* samples in the buffer (this condition happens only after a reset, a clear or after a *Full* condition), the trigger is either not accepted or, if it is still active when the *Npre* samples are all written in the buffer, accepted with a delay.

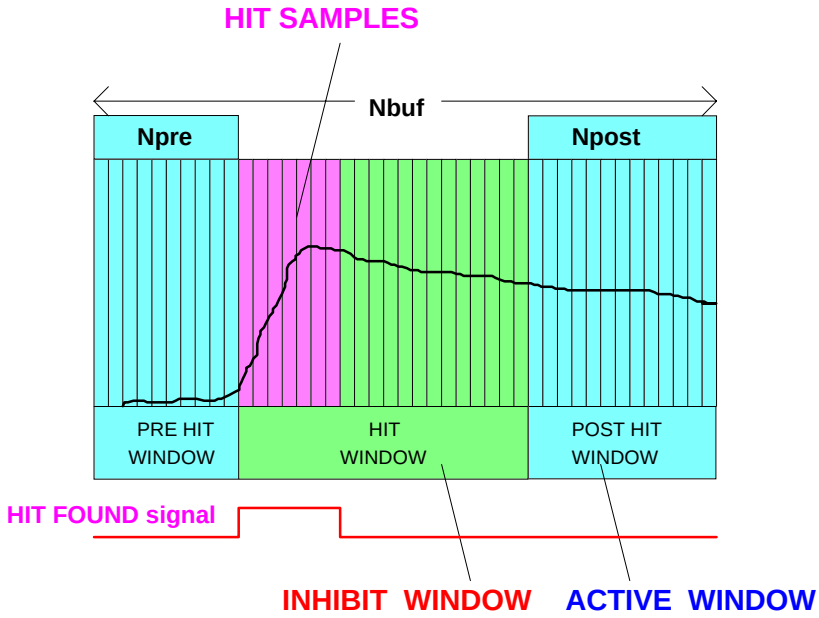


Fig. 3.7 - Pre-hit, post-hit and hit windows

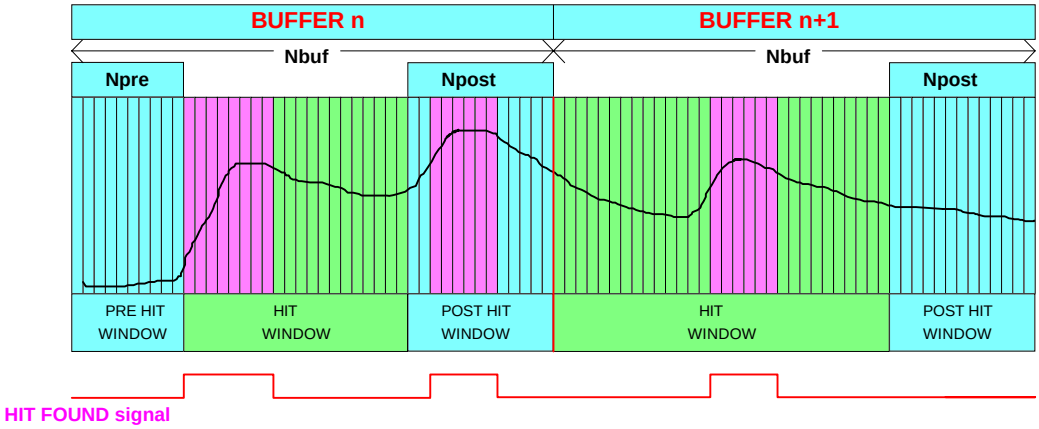


Fig. 3.8 - Trigger overlap

While the samples of the inhibit window are written, the trigger logic does not accept other trigger signals. At the end of this window, the presence of a trigger which is still active or the occurrence of a new trigger, causes the memorisation in a new buffer (*trigger overlap*, refer to Fig. 3.8). In this case it may happen that some of the *Npre* samples are contained in the previous buffer and, as a consequence, will not be memorised in the new buffer.
In the case of VME or external or global trigger signals, the trigger logic generates an internal signal of duration equal to the inhibit window: in this way it extends the duration of the trigger in order to force the acceptance of these kind of trigger signals, even if they start (and end) inside the inhibit window. This implies that the occurrence of an external or global trigger or a VME trigger during the storage of a buffer causes anyway the storage of a new buffer appended to the previous one.

To sum up, the functioning of the trigger logic can be outlined as follows:

- *after a reset command, a clear command or a Full condition, the logic waits for the condition in which there are at least Npre samples in the memory; during this phase the trigger signals are not accepted.*
- *as soon as the Npre samples are written, the presence of a still active trigger or the occurrence of a new one cause the memorisation of other Npre-Nbuf samples in the present buffer and, as the buffer is completed, the passage to a new one.*
- *while the Npre-Nbuf-Npost samples are written, no other trigger signals are accepted; this is because it is thought that the signal which has caused the further trigger is fully contained inside the inhibit window and, consequently, already memorised in the buffer. Conversely, in the case that the trigger is an external or global or VME one, it is kept active till the end of the present inhibit window and then accepted.*
- *after the end of the inhibit window or during the post trigger window, if there is a still active trigger or a new trigger, these cause the memorisation in another buffer following the previous one (trigger overlap).*

The Header FIFO contains a word indicating which channels have generated the trigger signals relative to the memorised buffer. This is performed by using the trigger mask: if during the write access to the buffer a PEAK line relative to a channel is set, the relevant bit of the trigger mask is kept set until it will be written in the Header FIFO. This means that, from the time in which the global trigger is set (start of the hit window) up to the end of the buffer (end of the post-hit window), 16 FLIP-FLOP (pattern latches) are enabled to be set to 1 and, if a PEAK line is set to 1, the relevant pattern latch will be set to 1. Please note that if the latch is set to 1, this value in the register must not be modified until the end of the buffer, i.e. until this register content is written in the FIFO. When a new buffer is to be written on, the latch must be set to 0. In case of trigger overlap the register is also reset during the passage to the new buffer, so if the trigger that caused the saving of a new buffer is completely contained within the previous buffer (BUFFER n in Fig. 3.8) the PEAK lines are set to 0 (unless a further trigger is still active after the Npre samples of the current buffer). Even if a trigger is generated and completely contained only inside the first Npre samples of the current buffer, which follows a buffer frozen, the PEAK lines are set to 0. This implies that all the bits of the trigger mask in the Header FIFO are zeros.

3.5.1 Parameters for the setting of the trigger logic

The trigger logic features the following parameters:

- ***Nbuf*** = Buffer size (64,128,256,512,1024,2048,4096);
- ***Npre*** = number of samples before the trigger;
- ***Npost*** = number of samples after the trigger;
- ***Nd*** = latency time of the DAEDALUS chip; as soon as the trigger relative to the samples n (referring to the time Tn) occurs, the samples n+Nd (referring to the time Tn + Nd) are being memorised in the circular buffer. (All the times are given in clock cycles).

Five registers control the operation of this logic:

Table 3.3 - Registers for the control of the trigger logic

Base + %10A8 or %20A8	Trig_c Register
Base + %10A6 or %20A6	Trig_b Register
Base + %10A4 or %20A4	Trig_a2 Register
Base + %10A2 or %20A2	Trig_a1 Register
Base + %10A0 or %20A0	Trigctr Register

In order to have the preferred operation mode of the trigger logic it is necessary to load, in a coherent way, the following values in the relevant registers:

- **Trig_c Register = Nbuf - Npost -2;**
- **Trig_b Register = Nbuf - Npre -Npost -Nd -4;**
- **Trig_a2 Register = Npre + Nd -1;**
- **Trig_a1 Register = Nbuf -3;**

The trigger control register allows to mask the various trigger sources and to set a threshold on the number of channels where a peak has been detected (MAJORITY Trigger). This threshold is set on the TRIGCTRL<7:4>.
The MAJORITY Trigger is generated (if enabled) as soon as the number of active PEAK<15:0> signals overcomes the threshold set on the TRIGCTRL <7:4>.
The meaning of the bits of this register is as follows:

Table 3.4 - Trigger control register

TRIGGER TYPE	bit<8>	bit<3>	bit<2>	bit<1>	bit<0>
Ext Trigger only	0	0	0	0	1
Ext Trigger + OR	0	0	1	0	0
Ext Trigger + MAJORITY	0	1	1	0	0
Ext Trigger + LEFT/RIGHT	0	0	0	1	0
Ext Trigger + OR + LEFT/RIGHT	0	0	1	1	0
Ext Trigger + MAJORITY + LEFT/RIGHT	0	1	1	1	0
Ext Trigger + VME TRIGGER	1	0	0	0	1

Please note that the bits TRIGCTR<7:4> contains the threshold for the MAJORITY TRIGGER.

3.6 Test mode

The V789 module has various testing modes which allow to check the connections of the internal buses and the correct functioning of the programmable logic devices, of the DAEDALUS chips and of the FIFO and RAM memories. In the figure below the buses involved in the various test procedures are shown.

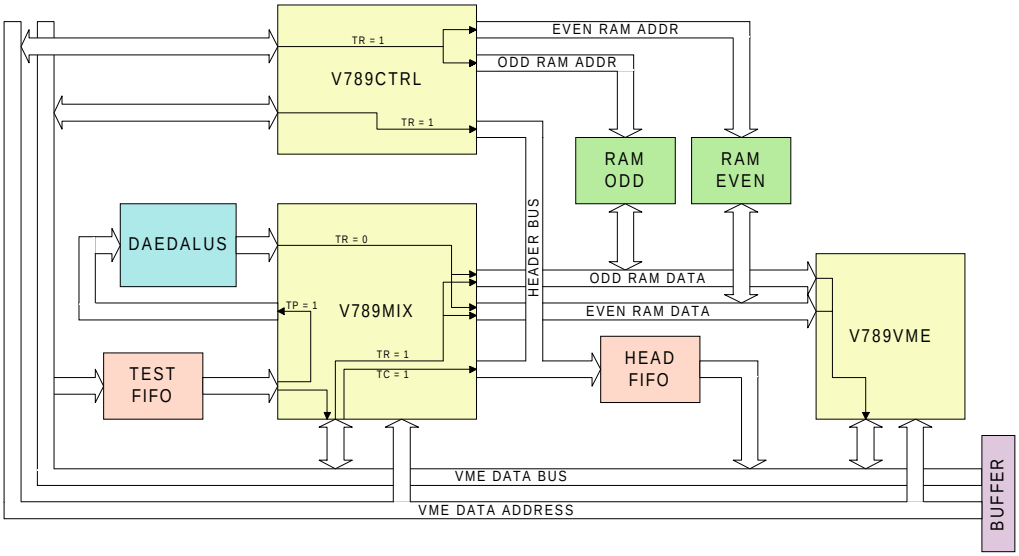


Fig. 3.9 - Buses involved in the test procedure

3.6.1 Test procedure for the RAM and the header FIFO

To enable this test mode the User must set the TR bit (bit 2) in the CTRL register. The purpose of this test mode is to verify the static RAMs constituting the MEB, the Header FIFO and the relevant data and address buses.
In this mode the RAM access does not depend anymore on the read and write pointers generated inside the module, but it occurs in RANDOM mode by using the VME Addresses (VAD). The write/read accesses are performed in D16 mode (in the space defined by VAD[21:18]) independently for the even and the odd part. In particular, VAD[17:2] correspond to the actual addresses of both the RAMs and VAD[1] defines the selected chip. As a consequence, this implies that:

- VAD[21:18] = 5: Block A (space %140000 - %17FFFE);
- VAD[21:18] = 9: Block B (space %240000 - %27FFFE);
- VAD[17:2] = RAM_ADDR[15:0];
- VAD[1] = 0: access to RAM EVEN;
- VAD[1] = 1: access to RAM ODD;

When a writing access is performed in RANDOM mode, the datum passes from the VME to the PLD V789MIX which makes them available on the data buses at the input of the two RAMs (odd and even). At this point the PLD V789CTRL gives the write command on the two RAMs in turn and, simultaneously, gives the strobe command to the PLD V789VME that writes the datum on its internal register devoted to the read out of the

MEB. The read operation can occur in two different ways: if a read operation in D32 mode is performed to the MEB address, the written datum is read directly in the VME interface without passing through the RAMs. In this case only half the 32-bit datum will be meaningful. If a read operation in D16 mode is performed in the RANDOM_RAM_SPACE, the written datum is read inside the RAM. The first type of read access allows to verify a correct connection of the PLD V789MIX and V789VME to the data buses of the RAMs; the second type of read access allows to verify as well the correct operation of the RAM chips and their correct connection to the data buses and addresses.

In this testing mode a writing access to the TEST HEADER register allows to force the write operation of a test header in the FIFO by following the same sequence used for the usual event header. The following 5 words are written:

- 1 16-bit word written by the VME interface;
- 1 fixed test pattern (0x5555);
- 3 words coming from the absolute time counter (32 bit in the whole) which, on the basis of the set-up of the TC bit of the CTRL register (refer to the following section for further detail), can contain either the absolute time value or a value written by the VME with test purposes.

This test procedure allows to verify the correct connection between the Header FIFO to the PLD V789MIX and V789CTRL and to the VME data bus together with the correct operation of the FIFO itself.

3.6.2 Test Counter

To enable this test mode the TC bit (bit 3) must be set in the CTRL register.
When this test mode is enabled, the 32-bit absolute time counter does not follow the ABS_CLK and RES_CLK signals coming from the P2 and PAUX connectors. The counter can be preset to a certain value by means of two writing accesses (16 bit + 16 bit) to the ABSOLUTE_TIME addresses (high and low). The preset value can be read as well at the same locations in order to verify the correct connection of the PLD V789MIX to the VME bus.
If the ABS_CLK signal is not running, the Header FIFO will not contain the preset test counter value unless a VME read access to the test counter (high and low) is performed. As a consequence, in this case the correct operation sequence is: writing the test counter value (high and low), reading it via VME and then writing the Test Header.
When this test mode is not enabled, the counter regularly performs its task and the present value can be read via VME by accessing to the same locations. This allows to verify the correct reception of the ABS_CLK and RES_CLK signals.

3.6.3 Test Pattern

To enable this test mode the TP bit (bit 4) of the CTRL register must be set.
This test mode allows to substitute the data coming from the link with the data contained in the Test Pattern FIFO (TPF). The purpose of this test operation is to verify the correct functioning of the whole acquisition logic and of the DAEDALUS chips.
The write operation of the test patterns is made via consecutive write accesses to the TEST_PATTERN address. The meaningful bits are the only first 10 bits. The TPF can contain up to 1024 data. A read access to the same address allows to read the test

pattern data written previously by passing through the PLD V789MIX: this allows to verify the correct connection of the TPF to the VME data bus and to the above mentioned PLD, together with the connection of the PLD to the VME data bus. The data which are read in this mode are then lost.
A write access to the RUN_TEST_PATTERN address allows to start the acquisition with the data contained in the TPF. The data are read from the TPF and sent to the mixer and to the DAEDALUS chips, in the same way as the data coming from the link. The only difference is that the data change every 16 clock periods instead of changing at each clock signal. This means that all the 16 channels of the both the blocks receive the same sequence of data.
As soon as the TPF has been emptied, the last datum is repeated until new test patterns are written and a new RUN command is given.

N.B.: the TEST pattern must be constituted by at least 2 words.

3.6.4 Reduced MEB

In order to allow test data acquisitions with a reduced number of data and to verify the behaviour of the system at the occurrence of the *Full* status, the possibility of programming the MEB with only two buffers of 8 samples each (64 long words) has been foreseen. The programmability of the MEB is enabled by writing '7' in the MODE register.

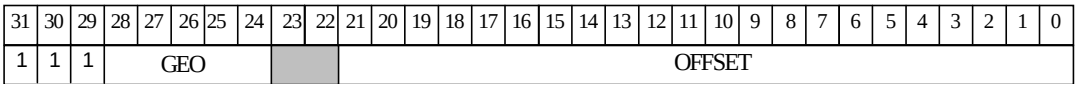
3.6.5 Internal CLOCK

To select the internal clock source the User must write '0' in the CK bit (bit 5) of the CTRL register. In this mode the board clock is generated by the local oscillator (40 MHz) and the SYNC signal is generated every 16 clock peaks by an internal counter. The SYNC signal, in this case, has no relation with the data flow.

4. SOFTWARE DESCRIPTION

4.1 Addressing Capability

The V789 module accepts both single and block transfer accesses in D32 mode only. Actually, the selection of the modules in the same crate is achieved by means of the only geographical address (read by the JAUX or by the J2 if the A873 board is present). This provides, by using 5 bits, the slot number occupied by the board. The GEO is mapped on the addresses (A[28:24]) and defines the module Base Address. In this way it completely substitutes the use of the rotary switches. The uppermost part of the addresses (A[29:31]) must be set to 1. The addresses have the following format:



Base Address [31:0] = %E000 0000 + (Geo Address [4:0] << 24)

Fig. 4.1 - Format of the V789 module addresses

The Address Modifier codes recognised by the module are:

AM=%0E	extended supervisor program access
AM=%0A	extended user program access
AM=%0D	extended supervisor data access
AM=%09	extended user data access
AM=%0F	extended supervisor block transfer
AM=%0B	extended user block transfer

4.2 Data Transfer Capability

The internal registers of the V789 module can be accessed in D16 mode, while the MEB can be accessed in D32 mode both with single access or block transfer mode. Since the MEB is modular (buffer with dimensions ranging from 64 to 4096 long words), a bus error generation at the end of the data is not foreseen during the block transfer access.

4.3 Interrupter

The V789 module, if enabled, can generate an interrupt request when the Data Ready is active. This request occurs at a fixed priority level (typically on the IRQ3 line). The level can be modified only via hardware by making an appropriate soldering on the printed board (please refer to Fig. 2.4).

4.4 Registers

4.4.1 Register Map

Table 4.1 - Address map for the V789 module

ADDRESS	REGISTER/CONTENT	TYPE
GLOBAL REGISTERS		
Base + %00	Control Register	read/write, D16
Base + %02	Test Pattern	read/write, D16
Base + %04	Absolute time (low)	read/write, D16
Base + %06	Absolute time (high)	read/write, D16
Base + %08	Software reset	write only, D16
Base + %0A	Interrupt Level	read/write, D16
Base + %0C	Interrupt Vector	read/write, D16
Base + %0E	Global Status	read only, D16
Base + %10	Clear Test Pattern	write only, D16
Base + %12	Run Test Pattern	write only, D16
Base + %14	Test Pattern Status	read only, D16
Base + %18	Dummy Register	read/write, D32
BLOCK A REGISTERS (CH 0..15)		
Base + %1000	Multi Event Buffer	read only, D32
Base + %1004	Status Register	read only, D16
Base + %1006	Header FIFO	read only, D16
Base + %1008	Mode Register	read/write, D16
Base + %100A	Increment Read Pointer	write only, D16
Base + %100C	Read Pointer	read only, D16
Base + %100E	Write Pointer	read only, D16
Base + %1010	Test header	read/write, D16
Base + %1012	Clear	write only, D16
Base + %1020	Reset DAEDALUS	write only, D16
Base + %1040 + DAEDALUS addr	DAEDALUS registers	read/write, D16
Base + %10A0	Trigctr Register	read/write, D16
Base + %10A2	Trig_a1 Register	read/write, D16
Base + %10A4	Trig_a2 Register	read/write, D16
Base + %10A6	Trig_b Register	read/write, D16
Base + %10A8	Trig_c Register	read/write, D16
Base + %10AA	Software Trigger	write only, D16
Base + %140000 + RAM addr	Test SRAM random access	read/write, D16

BLOCK B REGISTERS (CH 16..31)		
Base + %2000	Multi Event Buffer	read only, D32
Base + %2004	Status Register	read only, D16
Base + %2006	Header FIFO	read only, D16
Base + %2008	Mode Register	read/write, D16
Base + %200A	Increment Read Pointer	write only, D16
Base + %200C	Read Pointer	read only, D16
Base + %200E	Write Pointer	read only, D16
Base + %2010	Test header	read/write, D16
Base + %2012	Clear	write only, D16
Base + %2020	Reset DAEDALUS	write only, D16
Base + %2040 + DAEDALUS addr	DAEDALUS registers	read/write, D16
Base + %20A0	Trigctr Register	read/write, D16
Base + %20A2	Trig_a1 Register	read/write, D16
Base + %20A4	Trig_a2 Register	read/write, D16
Base + %20A6	Trig_b Register	read/write, D16
Base + %20A8	Trig_c Register	read/write, D16
Base + %20AA	Software Trigger	write only, D16
Base + %240000 + RAM addr	Test SRAM random access	read/write, D16

4.4.2 CTRL Register

(Base address + %00 read/write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										CK	TP	TC	TR	T1	T0

Fig. 4.2 - CTRL Register

T0,T1: DATA COMPOSITION

The <T1:T0> values determine the composition of the data, which is done by the mixer according to the table below:

Table 4.2 - Composition of the data

DATA BUS	T<1:0>=0 Normal	T<1:0>=1 DAEDALUS test	T<1:0>=2	T<1:0>=3
DT <0>	ADC <0>	F <0>	not used	not used
DT <1>	ADC <1>	F <1>	not used	not used
DT <2>	ADC <2>	F <2>	not used	not used
DT <3>	ADC <3>	F <3>	not used	not used
DT <4>	ADC <4>	F <4>	not used	not used
DT <5>	ADC <5>	F <5>	not used	not used
DT <6>	ADC <6>	F <6>	not used	not used
DT <7>	ADC <7>	F <7>	not used	not used
DT <8>	ADC <8>	F <8>	not used	not used
DT <9>	ADC <9>	F <9>	not used	not used
DT <10>	OR(F<4:0>)	0	not used	not used
DT <11>	F<5>	0	not used	not used
DT <12>	F<6>	0	not used	not used
DT <13>	F<7>	0	not used	not used
DT <14>	F<8>	0	not used	not used
DT <15>	F<9>	0	not used	not used

ADC<i> = i-th bit of the data coming from the ADC
DT<i> = i-th bit of the data at the SRAM input
F<i> = i-th bit of the data DAEDALUS chip output

TR: TEST RAM and HEADER FIFO

The value of TR (TEST RAM) determines the access mode to the RAM and to the Header FIFO as follows:

TR = 0 (Test RAM OFF): The RAM memory is paged. The data to be written come from the mixer. Write access is controlled internally, while read access is performed sequentially in D32 mode.
The pointers are internally controlled.
The Header FIFO contains the data relative to the events.

TR = 1 (Test RAM ON): The RAM memory is not paged. The data to be written come from the VME bus. Both write and read accesses are controlled via VME in Random mode and in D16 mode independently for the two RAMs, odd e even.
The pointers are substituted by the VME addresses.
The Header FIFO contains the test data.

TC: TEST COUNTER

The value of TC (TEST COUNTER) determines the operation mode of the absolute time counter as follows:

TC = 0 (Test CNT OFF): The absolute time counter is reset by the ABSRES signal and it is synchronised with the ABSCLK clock coming from the JAUX bus and from the J2 bus. The value of the counter can be captured via VME but cannot be written.

TC = 1 (Test CNT ON): The counter can be preset/read via VME by write/read access to the *Absolute Time* double register. In this mode the counter is not enabled.

TP: TEST PATTERN

The value of TP (TEST PATTERN) determines the source of the input data at the mixer and at the DAEDALUS chips as follows:

TP = 0 (Test PTN OFF): The data come from the link.

TP = 1 (Test PTN ON): The data come from the FIFO containing the test patterns.

CK: CLOCK SOURCE

The value of TC (CLOCK SOURCE) determines the source of the board clock as follows:

CK = 0 (internal CLK): The clock is generated by the internal oscillator and the SYNC signal (internally generated) does not have any meaning.

CK = 1 (external CLK): The clock comes from the link and the SYNC signal tags the channel 0.

4.4.3 TEST PATTERN Register

(Base address + %02 read/write)

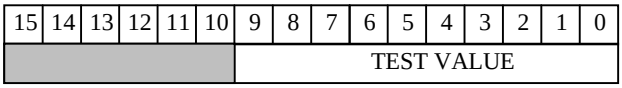


Fig. 4.3 - TEST PATTERN Register

A write access to this register allows to write a 10-bit value in the TEST PATTERN FIFO. The set of all the written values constitutes a test pattern which can substitute the data coming from the link. The maximum number of values contained in the FIFO is 1K. The TEST PATTERN must be constituted by at least 2 words.
A read access to this register allows to read the TEST PATTERN FIFO and verify it. The data which are read in this way are lost and are no more contained in the test pattern.

4.4.4 ABSOLUTE TIME Registers

(Base address + %04 (low value) read/write);
(Base address + %06 (high value) read/write);

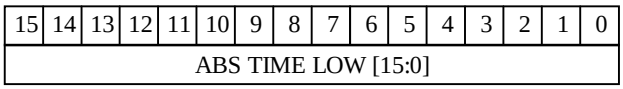


Fig. 4.4 - ABSOLUTE TIME Register [15:0]

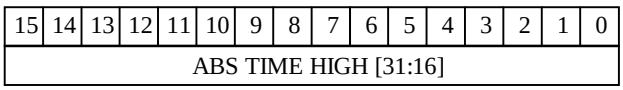


Fig. 4.5 - ABSOLUTE TIME Register [31:16]

When the TEST COUNTER mode is enabled (please refer to the Section 4.4.2), the write and read access to these two registers allows to set the value of absolute time and to read it, respectively. When the TEST COUNTER mode is not enabled, these registers can be only read and contain the present value of the absolute time.

4.4.5 Software RESET

(Base address + %08 write only)

A write access to this register allows to reset the module completely like Power-ON and SYSRES signals. In detail, the following tasks are performed:

- all the FIFO and memories are cleared;
- all the read/write pointers are set to zero;
- all the memory and trigger parameters are reset;
- the trigger logic is disabled;
- the interrupters are disabled;
- all the test modes are disabled;
- the internal clock is selected.

4.4.6 INTERRUPT LEVEL Register

(Base address + %0A read/write)

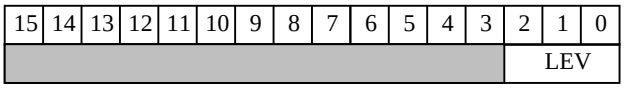


Fig. 4.6 - INTERRUPT LEVEL Register

This register contains the interrupt level. Since the level is not programmable via software but is cabled via hardware on a particular IRQ line, this register must contain the level corresponding to the used IRQ line. If the register contains a meaningless value, the interrupts are disabled.

4.4.7 INTERRUPT VECTOR Register

(Base address + %0C read/write)

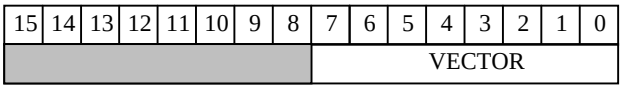


Fig. 4.7 - INTERRUPT VECTOR Register

This register contains the interrupt vector which is used during the interrupt acknowledge according to the VME standard.

4.4.8 GLOBAL STATUS Register

(Base address + %0E read only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													FF	DR	OF

Fig. 4.8 - GLOBAL STATUS Register

The bits of this register correspond to the logic OR on the corresponding bits of the STATUS registers of the two blocks A e B. The value of the bits in this register indicate the status of the relevant LEDs on the front panel (0 -> LED off; 1 -> LED on).

OF: **Overflow**
= 0 Neither of the DAEDALUS chips is in overflow;
= 1 At least one of the DAEDALUS chips is in overflow.

DR: **Data Ready (at least 1 whole buffer is in memory)**
= 0 Both the MEB are EMPTY;
= 1 At least one of the two MEB has some data;

FF: **Full**
= 0 Neither of the two MEB is FULL;
= 1 At least one of the two MEB is FULL.

4.4.9 Clear TEST PATTERN

(Base address + %10 write only)

A write access to this register deletes all the data contained in the test pattern FIFO.

4.4.10 Run TEST PATTERN

(Base address + %12 write only)

When the TEST PATTERN mode is enabled, a write access to this register allows to run the test pattern (the data are read by the FIFO and sent to the mixer and to the DAEDALUS chips by simulating a normal acquisition). When the FIFO is empty, the last datum is repeated until a new run command occurs.
The test pattern is common to all the 32 channels: this means that the data are read by the test FIFO at a frequency of 2.5 MHz and are then kept at the input of the two blocks A and B for 16 clock periods.

N.B.: the TEST PATTERN must be constituted by at least 2 words.

4.4.11 TEST PATTERN STATUS Register

(Base address + %14 read only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														FP	EP

Fig. 4.9 - TEST PATTERN STATUS Register

A read access to this register allows to gain information on the status of the test pattern FIFO.

EP: **Empty Test Pattern FIFO**
= 0 NOT EMPTY;
= 1 EMPTY.

FP: **Full Test Pattern FIFO**
= 0 NOT FULL;
= 1 FULL.

4.4.12 DUMMY Register

(Base address + %18 read/write, D32 only)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUMMY WORD																															

Fig. 4.10 - DUMMY Register

This register allows to write/read a 32-bit dummy word which can be used for test purposes.

+ +
NOTE: Please note that the registers described in the following are related to each of the two blocks and consequently occupy two different locations. They can be anyway written and read separately.
+ +

4.4.13 Multi Event Buffer

(Base address + %1000 or %2000 read only, D32 only)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ODD CHANNEL																EVEN CHANNEL															

Fig. 4.11 - Multi Event Buffer: locations for the odd and even channels

A read access in D32 mode to this location allows to read two samples relative to two adjacent channels (one even and the other odd) from the buffer. More consecutive read accesses or a block transfer operation allow to read sequentially all the samples contained in the present buffer. Once the end of the buffer is reached, the read out starts again from the beginning of the same buffer. In order to pass to the following buffer it is necessary to increment the pointer to the read buffer by means of a write access to the INCBRP register (Base + %100A or %200A).
Read accesses to this location when the MEB is empty cause the read out of meaningless data. It is up to the User to check the actual presence of data via the STATUS register before performing a read out of the MEB.
When the TEST RAM mode is enabled, accesses to this location allow to read directly the data written in the mixer for test purposes. It is anyway possible to pass from the TEST RAM mode to the normal mode and vice versa without loosing the data written in the memories.

4.4.14 STATUS Register

(Base address + %1004 or %2004 read only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									ET	OV	EH	FH	DR	AM	FM

Fig. 4.12 - STATUS Register

The status register gives information about the status of the MEB and of the Header FIFO.

FM: Full Multi Event Buffer
= 0 NOT FULL;
= 1 FULL.

AM: **Almost Full Multi Event Buffer (only 1 buffer is empty)**
= 0 NOT ALMOST FULL;
= 1 ALMOST FULL.

DR: **Data Ready (at least 1 buffer is full in the memory)**
= 0 MEB EMPTY;
= 1 Data Ready;

FH: **Full Header FIFO (for test purposes)**
= 0 NOT FULL;
= 1 FULL.

EH: **Empty Header FIFO (for test purposes)**
= 0 NOT EMPTY;
= 1 EMPTY.

OV: **DAEDALUS chip Overflow**
= 0 NOT OVERFLOW;
= 1 OVERFLOW.

ET: **Trigger Enable (read via PAUX or P2)**
= 0 trigger not enabled (except for the VME, external and global triggers);
= 1 trigger enabled.

4.4.15 Header FIFO

(Base address + %1006 or %2006 read only)

A read access to this register allows to read a 16-bit word from the Header FIFO. Each event written in a buffer of the MEB has a relevant header made of 5 words which have to be read sequentially (5 VME accesses in D16 mode) to this location. The data which constitute the headers can be read once only.

The Header contains the following informations:

The 12 bits of the Stop Pointer Address (pointer to the last sample);
The MODE bits which encode the type of mapping of the MEB;
The TV and TRCTRL bits which encode the trigger source;
The PEAK signals of the DAEDALUS chips (each bit is 1 if the relevant PEAK has been set at least once inside the trigger window);
The value of the absolute time corresponding to the last sample written in the buffer.

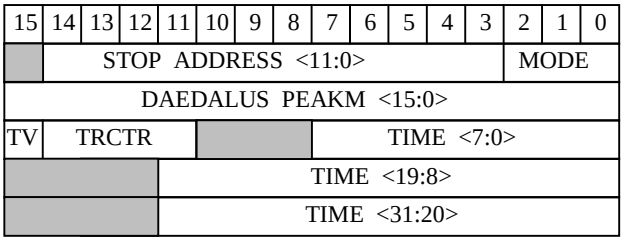


Fig. 4.13 - Header FIFO

The TV and TRCTRL bits are used to encode the trigger source, as indicated in Table 4.3.

Table 4.3 - Encoding of the trigger source via the TV and TRCTRL bits of the header

TV	TRCTRL	SOURCE
1	meaningless	VME
0	1000	Logic OR on the PEAK signals
0	0100	MAJORITY on the PEAK signals
0	0010	LEFT/RIGHT trigger
0	0001	External or global trigger

The STOP POINTER ADDRESS is used to rebuild the correct temporal sequence of the samples contained in the buffer. The total number ***Nw*** of long words of one buffer is given by the number of samples ***Nbuf*** times 8 (actually, each word contains the data of only two channels). Thus, the Stop Address times 8 gives the location of the word containing the last sample (in a temporal sense) relative to the channels 0 and 1. Consequently, the reconstruction of the buffer must start from the word given by:

((STOP ADDRESS * 8) + 8) mod (Nbuf * 8)

4.4.16 MODE Register

(Base address + %1008 or %2008 read/write)

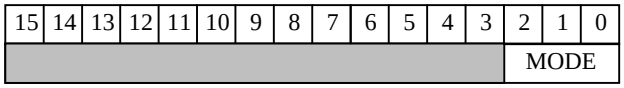


Fig. 4.14 - MODE Register

The value of the MODE register determines the type of MEB memory mapping according to the following table:

Table 4.4 - MODE register and MEB memory mapping

MODE	Nr. samples per buff., per ch.	Nr buffer	read/write pointer nr. bit
0	64	128	7
1	128	64	6
2	256	32	5
3	512	16	4
4	1024	8	3
5	2048	4	2
6	4096	2	1
7 (test mode)	8	2	1

4.4.17 INCREMENT READ Pointer

(Base address + %100A or %200A write only)

A write access to this register allows to increment the pointer to the read buffer. When the MEB is empty, an access to this register does not cause any change.

4.4.18 READ POINTER Register

(Base address + %100C or %200C read only)

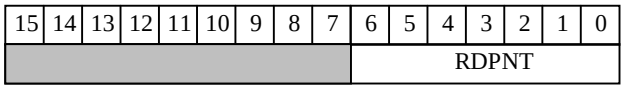


Fig. 4.15 - READ POINTER Register

A read access to this register gives the value of the Buffer Read Pointer.

4.4.19 WRITE POINTER Register

(Base address + %100E or %200E read only)

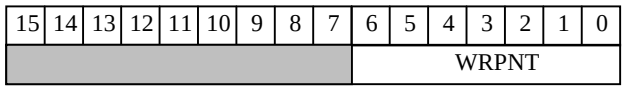


Fig. 4.16 - WRITE POINTER Register

A read access to this register gives the value of the Buffer Write Pointer.

4.4.20 TEST Header

(Base address + %1010 or %2010 read/write)

When the RAM TEST mode is enabled, a write access to this register allows to write a test header in the Header FIFO. The purpose of this task is to verify the connection to the data buses. The test header is constituted by five 16-bit words (like the real header) the first of which corresponds to the value passed during the write access via VME, the second one is 0x5555 and the last three ones give the value of the absolute time counter according to the setting of the COUNTER TEST (please refer to Sections 3.6.2 and 4.4.2). The test header can be read via VME in the same way as the event header are read.
A read access to this register allows to read the value written previously for test purposes.

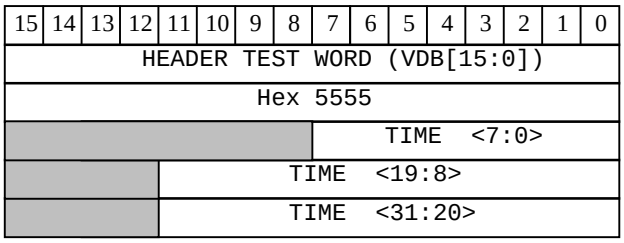


Fig. 4.17 - TEST Header

N.B.: the information written in the Header FIFO can be read only by 5 read accesses to the Header FIFO (refer to § 4.4.15 and Fig. 4.13). A read access to the TEST Header will allow to read only the Header TEST word.

4.4.21 CLEAR

(Base address + %1012 or %2012 write only)

A write access to this location allows to clear the stored data without resetting the settings. In other words, a CLEAR command causes the following tasks:

- the data contained in the MEB are cleared;
- the read and write pointers are set to zero;
- the Header FIFO is cleared;
- the trigger logic is initialised (without the loss of the settings).

4.4.22 Reset DAEDALUS

(Base address + %1020 or %2020 write only)

A write access to this location allows to reset the DAEDALUS chip.

4.4.23 DAEDALUS Registers

(Base address + %1040 ÷ %105A or %2040 ÷ %205A read/write)

The read and write accesses to this space allow to program the DAEDALUS chip. Each 16-bit word is to be regarded as divided into four 4-bit groups, each of which programs one of the four independent units which constitute the DEADALUS chip:

UNIT0 : channels[3:0]
UNIT1 : channels[7:4]
UNIT2 : channels[11:8]
UNIT3 : channels[15:12]

Here below a list of the DAEDALUS programming parameters (Table 4.5) is reported together with the list of the registers (Table 4.6).

Table 4.5 - Programming parameters of the DAEDALUS chip

Parameter name	Function
Digital_filter_size <3:0>	Number of time samples that defines the peak-search time interval.
Median_size <3:0>	Number of time samples used to calculate the median filter value.
Rising_sum_threshold <9:0>	Value of the positive differences sum inside the fixed time interval *above* which an peak is detected.
Falling_sum_threshold <9:0>	Value of the positive differences sum inside the fixed time interval *below* which the is considered detected.
Rising_zero_count <3:0>	Number of null differences counts inside the fixed time interval that are allowed in edges search.
Falling_zero_count <3:0>	Number of null differences counts inside the fixed time interval that are sufficient after a peak detection to consider the rising of the signal ended.
Rising_negative_count <3:0>	Number of negative differences counts inside the fixed time interval that are allowed in edges search.
Falling_negative_count <3:0>	Number of negative differences counts inside the fixed time interval that are sufficient after a peak detection to consider the rising of the signal ended.
Wire_cutting <3:0>	It masks peak detection of the specified channels: wire_cutting <n> = 0 forces PEAK <n> output to 0 wire_cutting <n> = 1 enables PEAK <n> output.
Polarity <0>	It defines whether falling or rising edges are searched: polarity = 0 for rising edges polarity = 1 for falling edges.

Table 4.6 - List of the registers of the DAEDALUS chip

Register	Address
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 P0 UNIT3 | P0 UNIT2 | P0 UNIT1 | P0 UNIT0	Base address + %1040 o &2040: P0 = Rising_sum_threshold <9:6>
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 P1 UNIT3 | P1 UNIT2 | P1 UNIT1 | P1 UNIT0	Base address + %1042 or %2042: P1 = Rising_sum_threshold <5:2>
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 P2 UN3 | P2 UN2 | P2 UN1 | P2 UN0	Base address + %1044 or %2044: P2 = Rising_sum_threshold <1:0>
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 P3 UNIT3 | P3 UNIT2 | P3 UNIT1 | P3 UNIT0	Base address + %1046 or %2046: P3 = Falling_sum_threshold <9:6>
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 P4 UNIT3 | P4 UNIT2 | P4 UNIT1 | P4 UNIT0	Base address + %1048 or %2048: P4 = Falling_sum_threshold <5:2>
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 P5 UN3 | P5 UN2 | P5 UN1 | P5 UN0	Base address + %104A or %204A: P5 = Falling_sum_threshold <1:0>
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 P6 UNIT3 | P6 UNIT2 | P6 UNIT1 | P6 UNIT0	Base address + %104C or %204C: P6 = Rising_zero_count <3:0>
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 P7 UNIT3 | P7 UNIT2 | P7 UNIT1 | P7 UNIT0	Base address + %104E or %204E: P7 = Falling_zero_count <3:0>
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 P8 UNIT3 | P8 UNIT2 | P8 UNIT1 | P8 UNIT0	Base address + %1050 or %2050: P8 = Wire_cutting <3:0>
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 P9 UNIT3 | P9 UNIT2 | P9 UNIT1 | P9 UNIT0	Base address + %1052 or %2052: P9 = Rising_negative_count <3:0>
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 P10 UNIT3 | P10 UNIT2 | P10 UNIT1 | P10 UNIT0	Base address + %1054 or %2054: P10 = Falling_negative_count <3:0>
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 P11 UNIT3 | P11 UNIT2 | P11 UNIT1 | P11 UNIT0	Base address + %%1056 or %2056: P11 = Median_size <3:0>
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 P12 UNIT3 | P12 UNIT2 | P12 UNIT1 | P12 UNIT0	Base address + %1058 or %2058: P12 = Digital_filter_size <3:0>
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 D | C | B | A	A = P13 UNIT0; B = P13 UNIT 1; C = P13 UNIT 2; D = P13 UNIT 3 Base address + %105A or %205A: P13 = Polarity <0>

4.4.24 TRIGCTRL Register

(Base address + %10A0 or %20A0 read/write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						ST	TV	MAJTH				CTR			

Fig. 4.18 - TRIGCTRL Register

A write access to this register allows to set the parameters for the trigger logic.

CTR (hardware trigger) and **TV** (VME trigger) encode the type of trigger source according to the following table:

Table 4.7 - TRIGCTRL register and the selection of the trigger source

TRIGGER TYPE	*TV*	*CTR<3>*	*CTR <2>*	*CTR <1>*	*CTR <0>*
Ext Trigger only	0	0	0	0	1
Ext Trigger + OR	0	0	1	0	0
Ext Trigger + MAJORITY	0	1	1	0	0
Ext Trigger + LEFT/RIGHT	0	0	0	1	0
Ext Trigger + OR + LEFT/RIGHT	0	0	1	1	0
Ext Trigger + MAJORITY + LEFT/RIGHT	0	1	1	1	0
Ext Trigger + VME TRIGGER	1	0	0	0	1

MAJTH defines the threshold for the Majority Trigger: if it is enabled, the Majority Trigger occurs when at least a number equal to MAJTH of PEAK signals coming from the DAEDALUS chip are active.

The **ST** bit allows to enable the trigger controller which manages the trigger logic and the data memorisation in the MEB and in the FIFO. After a reset or a Power ON, ST is set to 0 and the trigger controller is off. Before starting an acquisition it is necessary to set the preferred parameters and then enable the trigger controller by writing 1 in the ST bit.

4.4.25 TRIG_A1 Register

(Base address + %10A2 or %20A2 read/write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				TRIG_A1 PARAMETER											

Fig. 4.19 - TRIG_A1 Register

TRIG_A1 is a parameter for the trigger logic and corresponds to:

NBUF - 3

where NBUF is the buffer dimension (number of samples per channel) selected via write access to the MODE register.

4.4.26 TRIG_A2 Register

(Base address + %10A4 or %20A4 read/write)

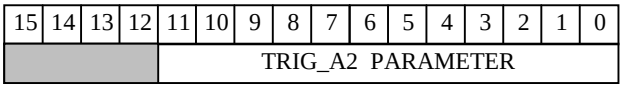


Fig. 4.20 - TRIG_A2 Register

TRIG_A2 is a parameter for the trigger logic and corresponds to:

NPRE + ND - 1

where NPRE is the number of PreTrigger samples and ND is the latency time of the DAEDALUS chip which depends on the window dimensions of the median filter and on the dimension of the peak research window.

4.4.27 TRIG_B Register

(Base address + %10A6 or %20A6 read/write)

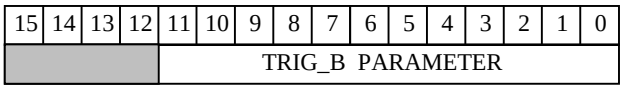


Fig. 4.21 - TRIG_B Register

TRIG_B is a parameter for the trigger logic and corresponds to:

NBUF - NPRE - NPOST - ND - 4

where NBUF is the number of samples per buffer, per channel, as set in the MODE register (refer to Table 4.4), NPRE is the number of PreTrigger samples, NPOST is the number of PostTrigger samples and ND is the latency time of the DAEDALUS chip which depends on the window dimensions of the median filter and on the peak research window dimensions.

4.4.28 TRIG_C Register

(Base address + %10A8 or %20A8 read/write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				TRIG_C PARAMETER											

Fig. 4.22 - TRIG_C Register

TRIG_C is a parameter for the trigger logic and corresponds to:

NBUF - NPOST - 2

Where NBUF is the buffer dimension (number of samples per channel) selected via a write access to the MODE register and NPOST is the number of PostTrigger samples.

4.4.29 Software Trigger (or VME Trigger)

(Base address + %10AA or %20AA write only)

A write access to this location allows to generate a software trigger. This is used for test purposes.

4.4.30 RANDOM RAM SPACE

(Base address + %140000 ÷ 17FFFE or %240000 ÷ 27FFFE read/write)

When the TEST RAM mode is enabled, the read/write accesses to this space allow to access to the RAM in RANDOM mode, that is without using read/write pointers controlled internally by the MEB control logic.
Read/Write access in D16 mode involves a single SRAM chip; the bit 1 of the VME Addresses (VAD) determines if the access is performed to the chip devoted to the even channels (VAD[1] = 0) or to that devoted to the odd ones (VAD[1] = 1). The VAD[17:2] bits directly constitute the 'physical' addresses of the two RAM chips.
Accesses to this location in normal mode have no meaning. It is anyway possible to pass from the normal mode to the TEST RAM mode and vice versa without loosing the data written in the memories.

5. REFERENCES

[1]. See for example the web site: *www.aquila.infn.it:80/icarus/*.

[2]. C.Carpanese *et al.*:"ARIANNA: the Icarus experiment readout module", *Proc. Of the Xth IEEE Real Time Conference*, Beaune, France, 22-26 September 1997, pp.299-303.

[3]. C.Carpanese *et al.*:"DAEDALUS: a hardware signal analyser for Icarus", *Proc. Of the 7th Meeting on Advanced Detectors*, Isola d'Elba, Italy, 25-31 May 1997 - *Nuclear Instruments and Methods*, A409/1-3, 1998, pp.294-296.

APPENDIX A

Software Examples

Software examples

Several software examples and test patterns for the V789 module can be downloaded from the FTP address: ftp://ftp.caen.it/pub/DocCaen/icarus/C_progs.