

Technical Information Manual

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MOD. V 793
ICARUS
SLOW CONTROL
MODULE

NPO:
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1. General description

1.1. Overview

The CAEN Model V793 board has been designed for the slow control, via either RS232 or CAENET communication path, of the analog crates into the ICARUS experiment acquisition chain. Each ICARUS analog crate can be equipped with a Mod. V793 and up to 19 Mod. V791 boards. The Mod. V793 main functions are:

- Generate the EN_BRD logic signals to enable/disable the Mod. V791 boards
- Set the acquisition baseline for the V791 boards
- Generate a clock signal to synchronise all the Mod. V791 boards in a crate
- Measure detector and crate power supply voltages
- Forward test pulses to the V791 boards, to the decoupling boards (Mod. A764) or to the detector during functional tests

Fig. 1.1 shows a detailed block diagram of the V793 module.

The Mod. V793 is housed in a 1-unit wide, 6 unit high Eurocard mechanics; please note that, although the module fits in a VME-like crate, the rear connectors are not VME standard connectors.

1.2. Block diagram

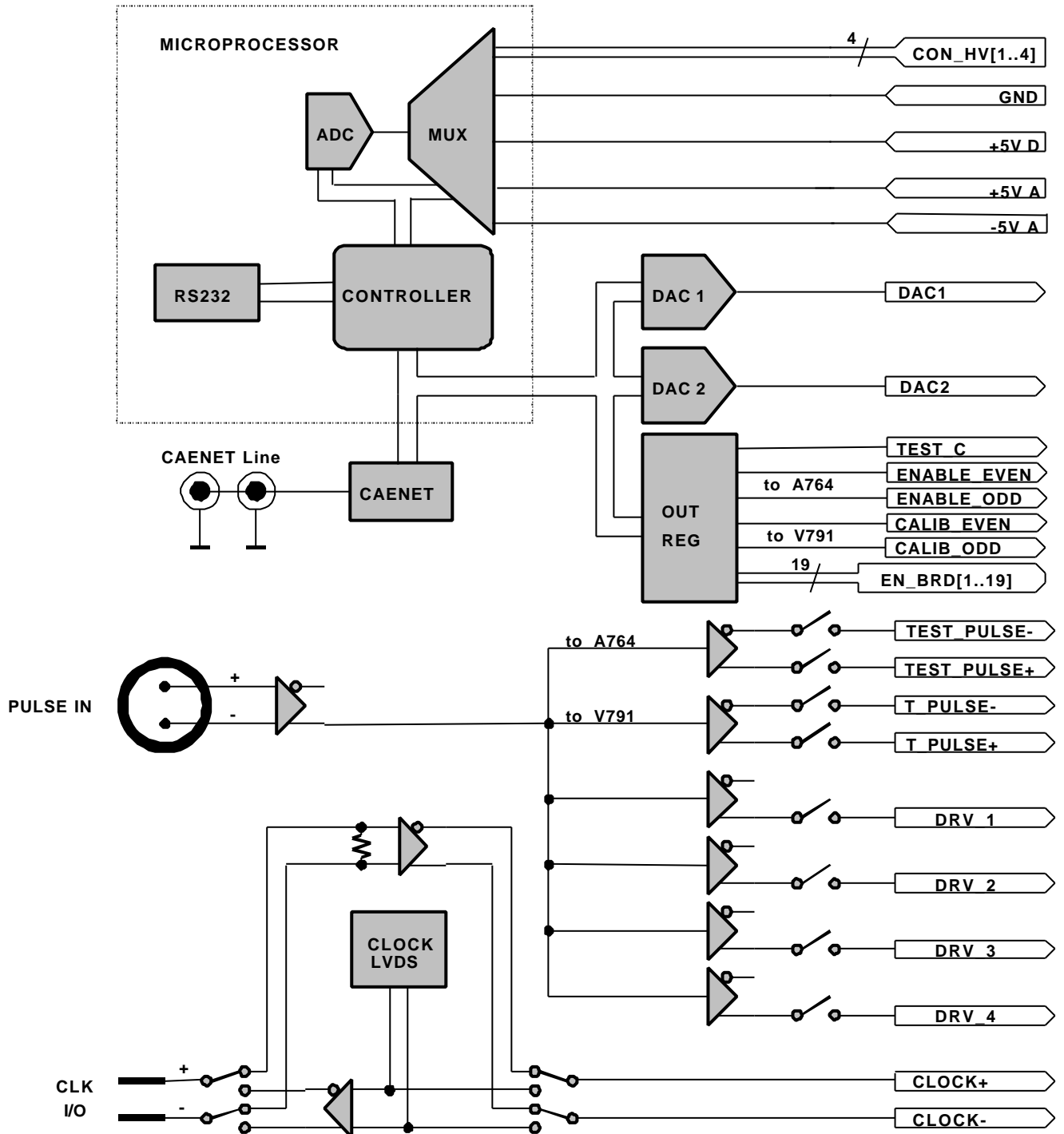


Fig. 1.1 - Block diagram of the Model V793

1.3. Functional description

1.3.1. Baseline generation

The Mod. V793 generates two DC voltage levels (DAC1 and DAC2) which allows to set the baseline acquisition for the V791 boards; the DC levels can be remotely programmed with 12 bit resolution on the 0÷+2.5 V range either via RS232 or CAENET interface. For each V791 board, it is possible to select the baseline (DAC1 or DAC2) according to the type of signal to be converted by acting on a backplane jumper.

1.3.2. EN_BRD signals generation

The Mod. V793 is able to generate the EN_BOARD[1...19] TTL signals which allow to enable/disable each of the V791 boards within an analog crate. If the EN_BOARD[n] signal is active, the n-th V791 board is forced into reset state and signal digitisation is stopped. The EN_BOARD signals can be remotely programmed either via RS232 or CAENET interface.

1.3.3. Clock signal generation

The Mod. V793 houses a 40 MHz quartz oscillator producing an LVDS differential clock signal CLOCK+/CLOCK-; this signal is employed to synchronise data acquisition on all the V791 modules in a crate. The clock signal can be also externally supplied via the front panel CLK I/O connector. The internal/external clock selection is performed through the JP8 jumpers (see § 2.6 for further details)

1.3.4. Detector and crate power supply voltages measurement

The Mod. V793 houses eight 8-bit ADCs dedicated to detector and crate power supply voltages measurement on the relevant backplane lines (see table below). The ADCs can be read out either via RS232 or CAENET interface.

Line	Range	Line	Range
CON_HV1	±2.5 V	GND	±0.5 V
CON_HV2	±2.5 V	+5 V	5±1 V
CON_HV3	±2.5 V	+5 V ANALOG	5±1 V
CON_HV4	±2.5 V	-5 V ANALOG	-5±1 V

1.3.5. Test pulses distribution

During functional tests, a differential test pulse (± 2.5 V range) can be injected into the V793 through the front panel PULSE IN connector (see block diagram at page 5); the pulse is splitted and then forwarded to the V791 modules or to the decoupling boards depending on the status of the CALIB_EVEN, CALIB_ODD, ENABLE_EVEN, ENABLE_ODD lines (TTL levels) as explained in the table below. The lines status is remotely programmable by RS232 or CAENET interface; four front panel LED (CE, CO, EE and EO) display the lines status. At module power-on test pulsing is disabled on all channels.

SIGNAL	ENABLE
CALIB_EVEN	=1 Test-pulse through T_PULSE lines (to V791 even channels)
CALIB_ODD	=1 Test-pulse through T_PULSE lines (to V791 odd channels)
ENABLE_EVEN	=1 Test-pulse through TEST_PULSE lines (on A764 even channels)
ENABLE_ODD	=1 Test-pulse through TEST_PULSE lines (on A764 odd channels)

Besides this, four remotely programmable lines (DRV_1...DRV_4) are available to send test pulses directly to the detector. The status of these lines is indicated by four front panel LEDs (DRV1...4).

2. Technical Specifications

2.1. Packaging

The board is housed in a 1-unit wide, 6-unit high Eurocard standard mechanics.
The front panel of the Model V791 is shown in Fig. 2.1.

2.2. Power Requirements

The power requirements of the board are:

Table 2.1 - Power requirements

<i>Power Supply</i>	<i>Absorption (max)</i>
+5 V digital	300 mA
+5 V analog	150 mA
-5 V analog	150 mA

The crate must have a low-noise linear power supply with separate analog and digital supply sections. It is suggested the use of a π -filter regulator for the analog section.

2.3. Front panel

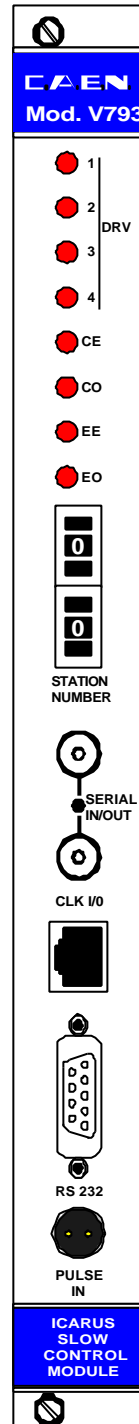


Fig. 2.1 - Model V793 front panel

2.4. External connections

2.4.1. Backplane connectors

The backplane connection pin configurations of the V793 module are shown in Fig. 2.2, while their function and electro-mechanical specifications are listed in the following sections.

BACKPLANE CONNECTOR P3

Mechanical specifications:

96-pin, C-type, A/B/C lines, DIN41612 standard connector;

Electrical specifications:

- **EN_BRD1... EN_BRD19:** enable signals for the V791 boards, TTL level;
- **ENABLE_EVEN,**
ENABLE_ODD test pulse enable signals for even (odd) A764 channels, TTL level;
- **CALIB_EVEN,**
CALIB_ODD test pulse enable signals for even (odd) V791 channels, TTL level;
- **CLOCK+, CLOCK-** differential clock signal, LVDS level;
- **TEST_PULSE+,**
TEST_PULSE- differential test pulse to A764
- **T_PULSE+,**
T_PULSE- differential test pulse to V791
- **AGND** analog ground;
- **DGND** digital ground;
- **+5V D** +5V for the digital section;
- **+5V A** +5V for the analog section;
- **-5V A** -5V for the analog section;
- **CON_HV1...CON_HV4** monitor lines for detector HV power supply, ± 2.5 V range;
- **TEST_C** TEST_C signal, TTL level
- **DAC1, DAC2** programmable baseline for the V791 boards

BACKPLANE CONNECTOR P1

Mechanical specifications:

32x2-pin, C-type, A/C lines, DIN41612 standard connector;

Electrical specifications:

- **AGND:** analog ground;;
- **DRV_1...DRV_4:** detector test pulses;

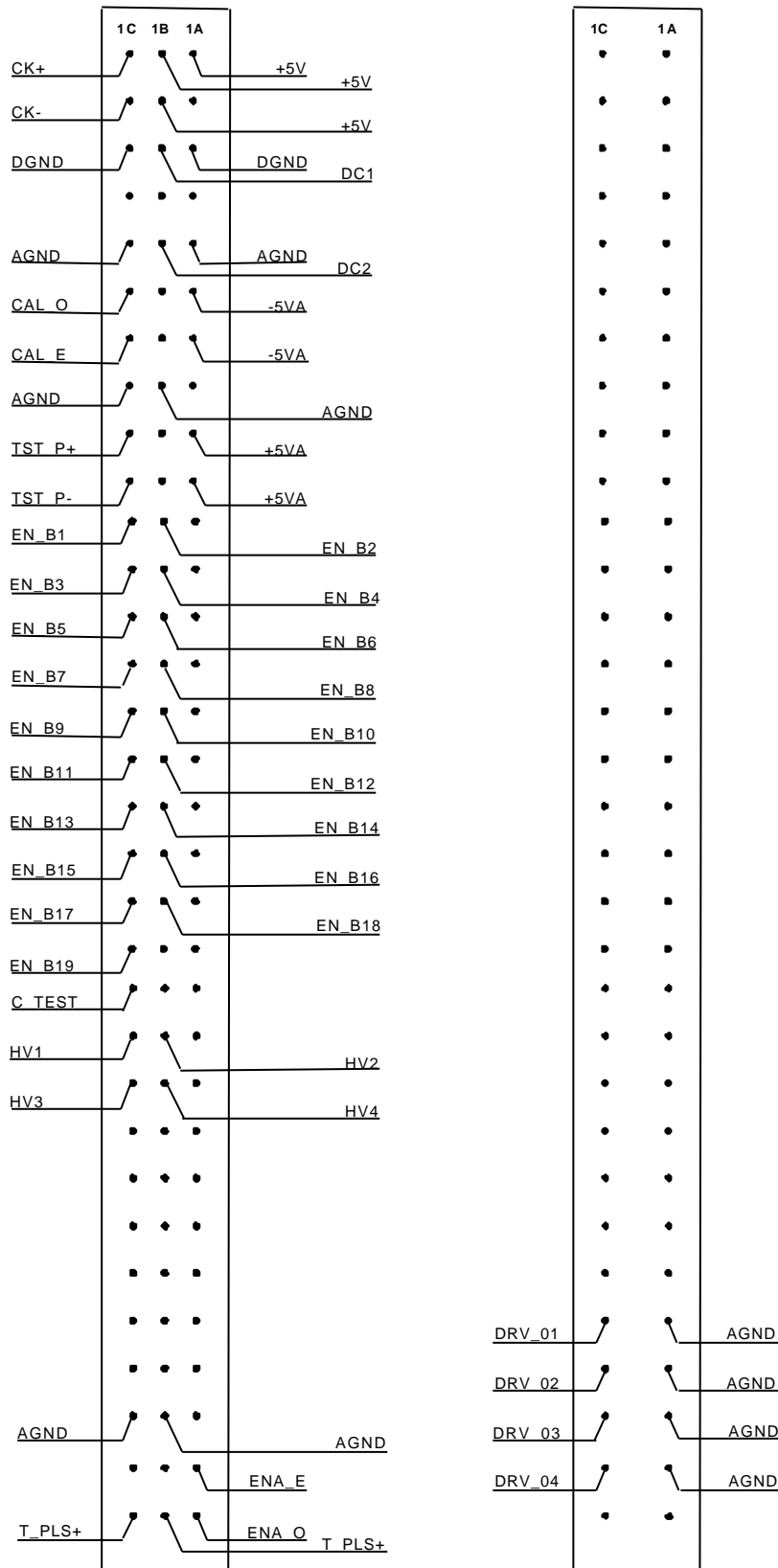


Fig. 2.2 - Pin configuration of Model V793 backplane connectors

2.4.2. Front panel connectors

SERIAL IN/OUT

Mechanical specifications:

two bridged LEMO 00 type connectors for daisy chaining;

Electrical specifications:

CAENET signals (see § 4 for further details)

CLK I/O

Mechanical specifications:

RJ45 type connector;

Electrical specifications:

LVDS 40 MHz clock signal

RS232

Mechanical specifications:

9 pin D-type connector;

Electrical specifications:

RS232 signals (see § 3 for further details)

PULSE IN

Mechanical specifications:

LEMO EPG 0B type connector;

Electrical specifications:

differential test pulse, ± 2.5 V range

2.5. Displays and switches

STATION NUMBER: 2 digit thumble switch

Function: it allows to select the CAENET station number.

CE: red LED.

Function: it lights up if the CALIB_EVEN line is active.

CO: red LED.

Function: it lights up if the CALIB_ODD line is active.

EE: red LED.

Function: it lights up if the ENABLE_EVEN line is active.

EO: red LED.

Function: it lights up if the ENABLE_ODD line is active.

DRV1...4 four red LEDs

Function: they light up if the relevant DRV line is active.

2.6. Jumpers

Please refer to Fig. 2.3 for jumpers location.

J8: CLK input termination

- Jumper between pin 2 and 3 \Rightarrow termination ON
- Jumper between pin 1 and 2 \Rightarrow termination OFF

JP3: clock configuration

- Jumper between pin 3 and 4 \Rightarrow the internal oscillator drives the CK+/CK- backplane lines
- Jumper between pin 5 and 6 \Rightarrow the external clock signal is sent to the CK+/CK- backplane lines

These two settings are mutually exclusive.

- Jumper between pin 1 and 2 \Rightarrow the internal oscillator drives the front panel CLK output
- Jumper between pin 2 and 4 \Rightarrow the clock signal on the CK+/CK- backplane lines is sent to the front panel CLK output.

These two settings are mutually exclusive.

JP1: RS232 port configuration

Two jumpers allow to exchange the TX and RX pins (see Fig. 2.4) according to the cable to be used.

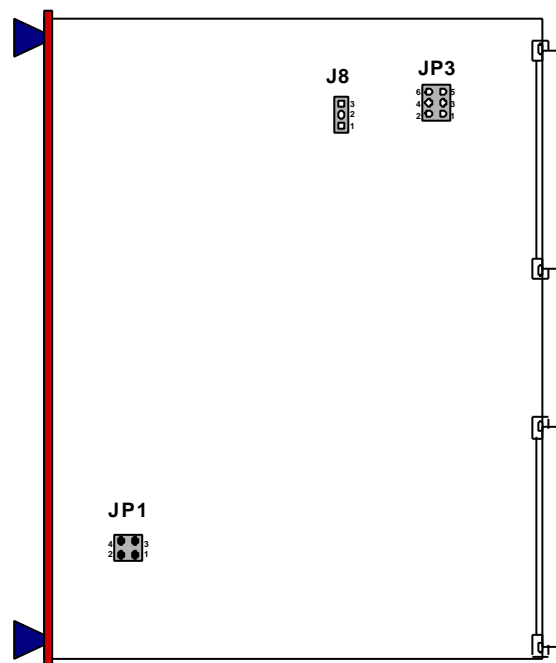
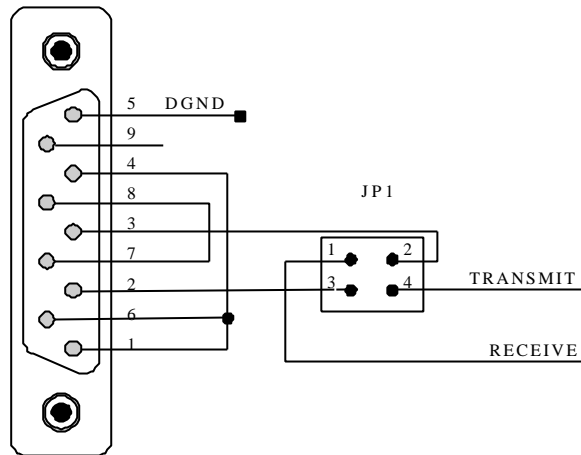


Fig. 2.3 - Jumpers location

**Fig. 2.4 – RS232 port configuration**

3. RS232 Interface

The Mod. V793 can be remotely controlled by a standard PC running a terminal emulator program via the RS232 port. The default settings of the RS232 interface are as listed in Table 3.1, while the RS232 pin assignment is given in Fig 2.2.

Table 3.1 – RS232 Port Settings

Baud rate	9600
Parity	None
Character length	8 bits
Number of stop bits	1 bit
Flow control	Xon/Xoff

Connect the V793 to the PC RS232 serial port (please refer to § 2.6 for TX/RX pin assignments) and then run the terminal emulator program. By sending a <CR> from the terminal, the V793 DACs values, the voltage measured by the ADCs on the CON_HV1...4, DGND, +5VA, +5VD and -5VA lines, the CAENET station number and the Enable, Test and DRV lines status will be displayed on the screen as illustrated in the figure below.

```

V793 Version 2.0
CON_HV1 = -1.44V  CON_HV2 = -1.50V  CON_HV3 = 0.96V  CON_HV4 = 1.02V
  DGND = 0.18V    +5VA = 5.18V    +5VD = 5.19V    -5VA = -5.63V

Enable board Status:
 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
OFF OFF OFF OFF OFF OFF OFF OFF OFF ON OFF OFF OFF OFF OFF OFF OFF OFF

Test Lines Status:
V791_E ON      V791_O OFF      A764_E OFF      A764_O OFF

DRV Lines Status:
DRV_1 OFF      DRV_2 OFF      DRV_3 OFF      DRV_4 OFF

DAC1 = 300      DAC2 = b00

Backplane C_TEST Disabled

CAENET Station Number: 31

Press Enter for new display, S for Setting Menu

```

Fig. 3.1 – DACs values and lines status with RS232

To modify any parameter, press the <S> key; the following Setting Menu will be displayed.

```
V793 Setting Menu

1 - Set Enable Board 1..19 hex <0..7FFFF>
2 - Set V791 Test Lines O-E hex <0..3>
3 - Set A764 Test Lines O-E hex <0..3>
4 - Set DRV Outputs 4..1 hex <0..F>
5 - Set DAC1 Output hex <0..FFF>
6 - Set DAC2 Output hex <0..FFF>
7 - Enable C_TEST Line <0/1>
T - Test Enable Lines
D - Test DAC1 & DAC2 Lines
```

Fig. 3.2 – V793 Setting Menu with RS232

- Press <1> to set the EN_BOARD lines status; write the pattern of inhibit (0...7FFFF hexadecimal) then press <CR>; the LSB corresponds to the EN_BRD1 line status.
- Press <2> to set the V791 test lines status; write the pattern of inhibit (0...3 hexadecimal) then press <CR>; the LSB corresponds to the CALIB_EVEN line status.
- Press <3> to set the A764 test lines status; write the pattern of inhibit (0...3 hexadecimal) then press <CR>; the LSB corresponds to the ENABLE_EVEN line status.
- Press <4> to set the detector test lines status; write the pattern of inhibit (0...F hexadecimal) then press <CR>; the LSB corresponds to the DRV_1 line status.
- Press <5> to set DAC1; write the DAC value (0...FFF hexadecimal) then press <CR>; FFF corresponds to +2.5 V.
- Press <6> to set DAC2; write the DAC value (0...FFF hexadecimal) then press <CR>; FFF corresponds to +2.5 V.
- Press <7> to enable/disable the TEST_C line ; write 1/0 then press <CR>
- Press <T> to test all the enable lines (front panel LEDs will light up sequentially); press <CR> to exit from the test.
- Press <D> to test DACs operation; the DACs will generate a saw tooth output between 0 and 2.5 V; press <CR> to exit from the test.

The DACs values and EN_BRD lines status set by the User are stored in memory after module power OFF.

4. CAENET Interface

Besides the RS232 interface, the V793 can be remotely controlled by a standard PC (with an A303A board installed) via CAENET interface. For details on the A303 board installation and operation, please refer to the *Mod. A303A High Speed CAENET PC Controller User's Manual*.

4.1. The V793 CAENET Controller

An example program (v793caenet.exe) is available from CAEN FTP site <ftp://ftp.caen.it/pub/DocCaen/icarus> to control the V793 via CAENET on Win platform. The v793caenet.exe program requires the A303A to be installed at I/O space address hex H280. The full v793caenet.exe source code is available from <ftp://ftp.caen.it/pub/DocCaen/icarus/v793caenet.zip>. For details on the CAENET commands format please refer to APPENDIX A.

Connect the V793 to the A303A on the PC via a 50 Ohm coaxial cable (the CAENET line needs to be terminated on the last board) and then run v793caenet.exe. Insert the CAENET station number according to the thumble switches setting on the module's front panel and then press OK; the V793 DACs values, the voltage measured by the ADCs on the CON_HV1...4, DGND, +5VA, +5VD and -5VA lines, the CAENET station number and the Enable, Test and DRV lines status will be displayed on the screen as illustrated in Fig. 4.1. To set any EN_BRD line status, simply click on the relevant box and then press the Set button; to set the DACs value, click on the relevant box and insert the desired value (hex) then press the Set button (FFF corresponds to +2.5 V). The DACs values and the EN_BRD lines status set by the User are stored in memory after module power OFF. The voltage measured by the ADCs on the CON_HV1...4, DGND, +5VA, +5VD and -5VA are displayed on the screen.

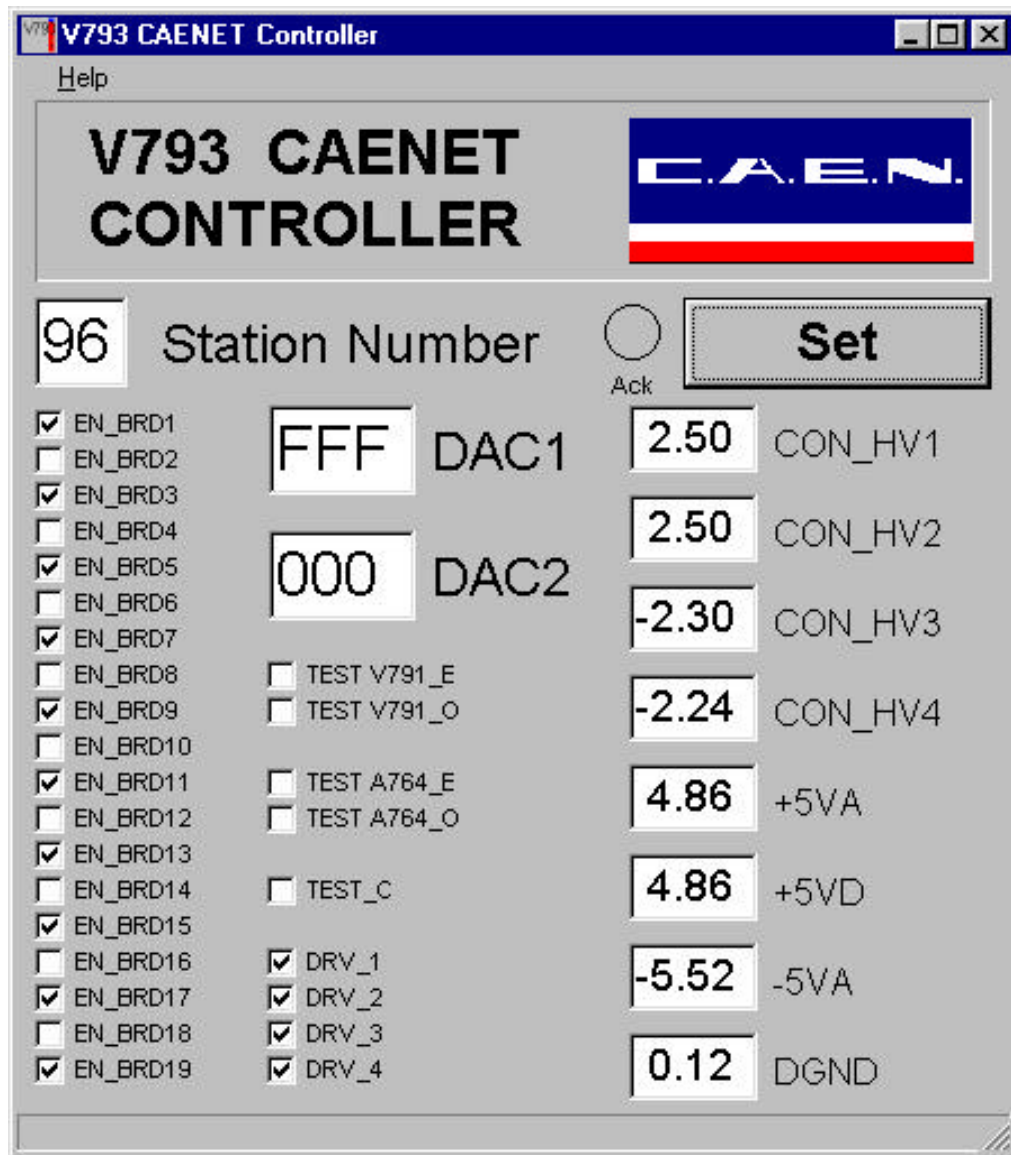


Fig. 4.1 – V793 CAENET Controller User Interface

APPENDIX A

Here follows a short description of the V793 status array bits and of the CAENET communication data packet exchanged with the Controller.

```

/*****/
/*
/* Meaning of the V793 STATUS array bits:
/*
/*MSB st.[0] st.[1] st.[2] st.[3] st.[4] st.[5] st.[6] st.[7] */
/* EN_B8 EN_B16 ENA_O DRV_1 DAC1_11 DAC1_7 DAC2_11 DAC2_7*/
/* EN_B7 EN_B15 ENA_E DRV_2 DAC1_10 DAC1_6 DAC2_10 DAC2_6*/
/* EN_B6 EN_B14 CAL_O DRV_3 DAC1_9 DAC1_5 DAC2_9 DAC2_5*/
/* EN_B5 EN_B13 CAL_E DRV_4 DAC1_8 DAC1_4 DAC2_8 DAC2_4*/
/* EN_B4 EN_B12 C_TEST - CNT_1 DAC1_3 CNT_1 DAC2_3*/
/* EN_B3 EN_B11 EN_B19 - CNT_0 DAC1_2 CNT_0 DAC2_2*/
/* EN_B2 EN_B10 EN_B18 - - DAC1_1 - DAC2_1*/
/*LSB EN_B1 EN_B9 EN_B17 - - DAC1_0 - DAC2_0*/
/*
/* EN_BRD bits are active low
/*
/*****/

/*****/
/*The message sent from the CAENET Controller has the format:
/*
/* MASTER IDENT. 1
/* CRATE NUMBER XX
/* OPERATION CODE:
/* byte high byte low
/* 0 0 -> module identification
/* 0 1 -> set V793 status
/* 0 2 -> get V793 status
/*
/* Code 0 1 is followed by these bytes:
/*
/* ADC[0] status[0] -> en_brd 8..1
/* ADC[1] status[1] -> en_brd 16..9
/* ADC[2] status[2] -> A764_0-E V791_0-E C en_brd 19..17
/* ADC[3] status[3] -> DRV_1..4 X X X X
/* ADC[4] status[4] -> DAC1_11..8 CNT1 CNT0 X X
/* ADC[5] status[5] -> DAC1_7..0
/* ADC[6] status[6] -> DAC2_11..8 CNT1 CNT0 X X
/* ADC[7] status[7] -> DAC2_7..0
/*
/* ANSWER CODE: 0 -> OK
/* FF00 -> module busy
/* FF01 -> wrong code or incorrect message
/*
/* Code 0 2 gives back the bytes sequence indicated above
/* preceded by the answer code
/* CNT1 enables test pulsing on the V791

```



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```
/* CNT0 enables test pulsing on the A764 */  
/*****/
```