

# Single Event Effects Measurements on the Electronics for the CMS Muon Barrel Detector at LHC

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## *Abstract*

Several irradiation tests of the electronics of the CMS barrel muon detector were performed using neutrons, protons and heavy ions. The Single Event Upset rate on some tested devices was measured, while upper limits were obtained for devices having experienced no failure.

Single Event Transients on front-end electronics and destructive effects on the HV distribution electronics were observed.

Overcurrent protection and error correction circuits were included in the irradiated boards and were tested.

## 1. Introduction

The LHC detectors will be working inside the highest radiation field ever experienced in high energy physics. Past studies were dedicated to the verification of the total radiation dose tolerance of the detector itself and its associated electronics.

However in certain locations of the detector the radiation dose absorbed in several years of operation is negligible and the expected particle fluence is not high enough to generate a important bulk damage. Nevertheless the detector electronics could still be disturbed or even damaged because of rare Single Event Effects (SEE) induced by interaction of the particles with silicon die.

Most of the barrel muon electronics of CMS [1] is located within the cavern, placed on the drift chambers or on the detector periphery, where the particle fluence in 10 years of LHC operation is below  $3 \times 10^{10} \text{ cm}^{-2}$  and the absorbed radiation dose is less than 0.2 Gy.

We expect that the reliability of the electronics will be associated with the probability of occurrence of SEE, usually considered only when designing aerospace instrumentation. Indeed access to the chambers buried inside the detector is granted only after several months of operation and in the detector periphery, even if more frequent, it is limited because of radiation protection rules.

## 2. Background Expectations

The CMS barrel muon chambers surround the calorimeters and are embedded in the iron yoke as shown in Figure 1. They are therefore shielded against the effects of charged low energy particles coming from the detector center. In addition they are located at several meters from the beam line and protected by the forward muon detector walls from secondary emissions due to beam halo interactions with magnets on the LHC transport line and with the CMS detector itself. Hence, as expected, simulation studies [2] showed that inside the muon barrel detector the background particle flux will be dominated by neutrons (Table 1).

Only a negligible fraction of the neutron flux will undergo non-elastic collisions, while all the others will thermalize within the cavern. We can safely assume that in a very short time they will form a pervasive neutron gas with an approximate flux of  $500 \text{ cm}^{-2} \text{ s}^{-1}$

The neutron background spectra obtained from the simulation are shown in Figure 2 for the two most important positions of the muon chambers. We see that the neutron flux is decreasing with energy and ends around 100 MeV in the outermost station (MB4) and at few hundred MeV in the innermost one (MB1). The latter is affected by higher energy neutrons due to spallation reaction products flooding through the CMS calorimeters and coil.

## 3. Single Event Effects Phenomenology

Single Event Effects are associated with the action of individual particles and their rate of occurrence is given as a cross section.

The most likely common effect is called Single Event Upset (SEU) and affects all kinds of memory devices (SRAM, DRAM and FLASH memories, microprocessors and DSPs, FPGAs and logic programmable state machines, etc.). It is detected as a modification of the memory state and is usually recoverable by data rewriting. Memory upset is caused by the deposition, inside a device sensitive node, of a charge higher than a given threshold. This charge value is dependent on both technology and device layout [3]. Even system architecture plays a relevant role in SEU

sensitivity: a careful system design helps in reducing the probability of device damaging as a by-product of a SEE [4][5]. Critical data can be protected either using less sensitive technologies or implementing redundant logic. Occasionally the energy deposition associated to the interacting particle can induce a latch-up (SEL), causing a block of the device sometimes recoverable by reset. Some effects are destructive and cannot be recovered: indeed the particle can induce a gate rupture (SEGR) or even a device burnout (SEBO)[6]. Both SEL and SEBO effects can be reduced by system architecture design: while the permanent damage associated to SEL can be eliminated using power supply and input-output overcurrent protection circuitry, the power device burnout probability can be reduced limiting the operating voltage to a fraction of the breakdown value. The least important effect is the Single Event Transient (SET) that generates noise inside charge sensitive devices (amplifiers and charge integrators). Its effect is device threshold dependent and only increases the natural noise of the device.

All the measurements carried out until now confirm that the SEU probability depends both on the integrated circuits technology and on the production process actually used in the factory. The associated technological parameters are usually not well controlled since two orders of magnitude in the published SEU cross section results are a typical variation.

Table 2 reports a list of the lowest energy open channels for the reaction  $n + {}^{28}\text{Si}$  [7]. Fast neutrons interact with  ${}^{28}\text{Si}$  atoms producing significant recoil energy already at neutron energy about 0.1 MeV[8]. The neutron elastic scattering with Si nuclei gives a negligible contribution to SEUs [9] and it must be considered only when verifying device tolerance to radiation dose. Therefore only non-elastic processes give a measurable probability. The total non-elastic cross section is reported in Figure 3. Only neutrons with an incident energy higher than 3 MeV contribute to the SEU measured cross section: the lowest energy reactions are in fact  ${}^{28}\text{Si}(n,p){}^{28}\text{Al}$  with a 4 MeV threshold and  ${}^{28}\text{Si}(n,\alpha){}^{25}\text{Mg}$  with a 2.7 MeV threshold: the cross sections for threshold reactions for incident neutron energy below 20 MeV are shown in Figure 4 [7]. The non-elastic cross-section reaches its maximum around 10 MeV and after that it slowly decreases. Furthermore the  ${}^{28}\text{Si}$  recoil energy saturates around 20 MeV neutron energy [10]. Hence SEU cross section is expected to have an energy threshold and should slowly increase with energy up to a saturation value. Neutron interaction with the plastic of the device package can occasionally extract protons that can be detected even below the energy threshold.

Recent tests [8] proved that thermal neutrons also cause SEU. The responsible mechanism is neutron capture from the  ${}^{10}\text{B}$  isotope (19.9% of natural boron), normally present in semiconductor technologies as a result of doping and in the glass passivation layer, followed by nucleus de-excitation with  $\alpha$ -particle emission through the reaction  ${}^{10}\text{B}(n,\alpha){}^7\text{Li}$ . Both the lithium nucleus and the  $\alpha$ -particle release locally enough energy to cause the memory cell change of state and the cross section is very large (3837 barn at 0.025 eV neutron kinetic energy). We found clear evidence of this mechanism using a windowless silicon photodiode (Hamamatsu S3590-02) as target and recording its signal. The energy spectrum of the particles produced by thermal neutrons interacting with the photodiode is shown in Figure 5. The three lines show the positions of full energy deposition in the depleted zone (2.31 MeV),  ${}^7\text{Li}$  deposited energy (0.8 MeV) and  $\alpha$ -particle deposited energy (1.5 MeV). Since the ranges in silicon of the  ${}^7\text{Li}$  fragment and of the  $\alpha$ -particle are respectively 2.5  $\mu\text{m}$  and 5  $\mu\text{m}$ , and the thickness of the depletion layer is about 20  $\mu\text{m}$ , the probability of partial energy deposition is not negligible. Such events are observable in the structures at the left of the 2.31 MeV peak. The spectral shape of these events is due to the distribution of the energy deposited along the track of the reaction products, which is not uniform.

Since neutron and proton non-elastic cross-sections are very similar for energies higher than 20 MeV (see Figure 3), it was stated that fast protons beams, more easy to find and manage,

could be used to qualify components to be operated with considerable neutron fluxes [2]. However different cross sections for secondary particle production by neutrons and protons must be taken into account. Furthermore the direct ionization of the proton irradiations somewhat modifies the SEU cross section measurements and induces total dose effects that are not likely to appear in a neutron irradiation. In particular the total dose effects inevitably connected to proton radiation tests were considered responsible for observed “data imprinting” effects (i.e. the devices cannot be reprogrammed and some random data is fixed in the memory location), frequently leading to underestimated values of the SEU cross-section [11].

#### 4. Measurements setup

CMS barrel muon detector electronics will be exposed to a wide spectrum of neutron energies. Our irradiation tests evaluate effects due to thermal neutrons and fast neutrons separately in the energy ranges below 10 MeV and  $20 \text{ MeV} \leq E \leq 60 \text{ MeV}$ .

Low energy neutrons are copiously produced in the nuclear laboratories by scattering of protons or deuterons on low atomic mass nuclei targets.

At the nuclear INFN laboratory of Legnaro (LNL, Italy) a deuteron beam accelerated up to 7 MeV by a Van de Graaff accelerator interacts with a thick beryllium target producing neutrons through the reaction  ${}^9\text{Be}(d,n){}^{10}\text{B}$ . The emitted neutron spectrum [12][13] is shown in Figure 6a for several incident deuteron energies. The neutron spectra high-end is limited to about  $E_n = 11 \text{ MeV}$ .

The Université Catholique of Louvain-la-Neuve laboratory (UCL, Belgium) provides a facility for a wide neutron spectrum using the reaction  ${}^9\text{Be}(p,n){}^9\text{B}$ , with a maximum incident proton energy of 65 MeV optionally cleaning the neutrons with a polyethylene/iron filter. The spectrum in our test setup is shown in Figure 6b: the energy distribution of the produced neutrons is roughly flat in the range 20-60 MeV.

Thermal neutrons were generated at LNL using the  ${}^9\text{Be}(d,n){}^{10}\text{B}$  reaction. The moderator [14][15] is sketched in Figure 7. The beryllium target is enclosed in a heavy water tank surrounded by very thick graphite walls. The fast neutrons produced in the d-Be scattering are therefore moderated by the heavy water and reflected from the graphite, thermalizing and remaining inside the graphite. The irradiation cavity is situated on top of the heavy water tank in a backward position with respect to the beryllium target in order to minimize the residual fast neutron content. The thermal neutron flux ( $E < 0.4 \text{ eV}$ ) is one order of magnitude larger than the epithermal neutron flux ( $0.4 \text{ eV} < E < 10 \text{ keV}$ ) and two orders of magnitude larger than the fast neutron flux ( $E > 10 \text{ keV}$ ). Since the neutron flux inside the graphite is modified by the inserted boards, we had to get the actual thermal neutron flux by comparison of the activation of indium and cadmium-indium targets placed just in front of each tested device: the thermal component is discriminated thanks to the high cadmium capture cross section for neutrons with energy below 0.4 eV. A further test was done on a thermal neutron column at the TAPIRO reactor at the Italian National Laboratories of ENEA at Casaccia (Rome).

UCL provides also a proton irradiation facility. Tests with protons at 60 MeV were done as a standard validation procedure foreseen for CMS. In most of the cases, the proton fluence was limited to  $5 \times 10^{10} \text{ cm}^{-2}$ , equivalent to a 70 Gy dose, in order to reduce total dose effects.

The tests were done in the period 1999-2001 on ASIC prototypes and commercial electronics considered to be sensitive to SEE.

In order to identify the SEU cases, device registers were initialized with a standard pattern, verified by the readout system with a cycle much shorter than the time between SEUs. Every time an alteration of the memory state was detected, the time, the integrated current on the target, the address and the datum were stored on disk for data analysis. In order to identify other

SEE the device currents were monitored during data taking and a device test was done after irradiation.

## 5. SEU cross section measurements on memory devices

Several kinds of memory device are included in the boards used in the CMS barrel muon electronics. Those tested are listed in Table 3: several devices of the same type and lot were irradiated. The total neutron fluence was  $\sim 10^{11} \text{ cm}^{-2}$  for thermal neutrons,  $\sim 10^{12} \text{ cm}^{-2}$  for fast neutrons and  $\sim 5 \times 10^{10} \text{ cm}^{-2}$  for protons.

The most sensitive devices happened to be Static RAMs: Figure 8 shows a plot of the SEU total number versus the neutron fluence for the SONY SRAM as an example of the data quality. The fact that the results are linearly distributed is an indication that there are no total dose effects, i.e. no saturation due to device degradation. The slope of the line fitted in this plot is a measurement of the SEU cross section of the device.

The large SEU probability found for SRAM devices allowed a more systematic study of the SEU phenomenon.

### 5.1 Search for a threshold

As already stressed there is an expectation of an energy threshold for fast neutrons induced SEU cross section. The known neutron reactions indicate that this threshold should be in the few MeV region (Table 2). As evidenced by the energy spectra of Figure 6a, the neutrons produced in the  ${}^9\text{Be}(d,n){}^{10}\text{B}$  reaction are not monochromatic. Measurements with thick beryllium targets using different incident deuteron energy are nonetheless useful to give an indication of the existence of a threshold, since the fraction of neutrons with  $E_n > 1 \text{ MeV}$  in the production spectra is quite different as a function of the deuteron beam energy.

Figure 9 shows the SEU cross section, for both the tested SRAMs as a function of the incident deuteron energy. The cross section was evaluated considering an equal contribution from all neutrons produced. Its behaviour for both RAMs is consistent with the existence of a threshold around  $E_n = 3 \text{ MeV}$ , as determined folding this distribution with the spectra of Figure 6a. We used the MCNP Montecarlo code [16] to determine the neutron flux and spectra expected through our devices with a careful description of the setup area in order to account for neutrons scattering on the walls, the floor and on the instrumentation inside the measurement area. This result agrees with the thresholds of the  ${}^{28}\text{Si}(n,p){}^{28}\text{Al}$  and  ${}^{28}\text{Si}(n,\alpha){}^{25}\text{Mg}$  reactions and the rising of the non-elastic neutron cross section. Therefore only thermal neutrons and fast neutrons with energy greater than roughly 3 MeV should be considered when computing device reliability against SEE. The contribution below the 3 MeV threshold should be caused by the protons extracted from the plastic of the device package.

### 5.2 Device response uniformity

Several SRAMs of the same type were tested in order to verify the uniformity of the device response. The results are collected in Table 4 showing a clear dependence on the neutron energy of the SEU cross section.

Furthermore the SEU probability of the tested devices varies by two orders of magnitude, but most of the measurements are within a factor two that could be regarded as a reasonable spread on device sensitivity to neutron irradiations. The found spread suggested the choice of a redundant system. In fact the final architecture uses three identical SRAM modules: each bit of any instruc-

tion is simultaneously read or written in all the memories; a majority logic coded within the ALTERA FPGA controls the read operation correcting for unmatching bits.

Another interesting check is scalability of measurements done at different energies and with different probes. Some of these devices were tested in a few conditions. In particular two SONY SRAMs were tested with neutrons at different energies and three TOSHIBA SRAMs were tested with neutrons and protons. The measurements are reported in Table 5: roughly the same scaling factor applies between tests with neutrons with  $3 < E_n < 11$  MeV and neutrons with  $20 < E_n < 60$  MeV or protons at 60 MeV energy. Therefore measuring with protons at 60 MeV, as foreseen as a standard test from CMS, and scaling with this factor, should provide the correct reliability figures for the tested devices within a factor two.

This scaling argument cannot in principle be applied to the thermal neutron effects, that should be more dependent on actual boron doping content and passivation layer composition for different factories, but again the scaling factor is roughly the same within a factor two and our result could be regarded as a sensible first guess for thermal neutron SEU cross sections on commercially available products.

### 5.3 Comparison between devices

SEU sensitivity was shown by microprocessor, TRACO and TSS ASICs at the highest incident particle energy, while all the other devices did not experience any failure. A small sample of these devices was measured showing a cross section spread within the average factor two already pointed out for the SRAM chips. Table 6 reports the results for the worst of the devices and a SEU cross section limit at 90% confidence level for the devices that did not show SEUs. A comparison between devices can be done by comparing the SEU probability per bit. Most devices relying on static RAM technology have a SEU cross section/bit of the order of  $10^{-14}$  cm<sup>2</sup>, while other devices are essentially SEU insensitive. In particular the ACTEL FPGA is built with antifuse technology (pASIC) and proved also to be radiation resistant.

## 6. SEE on front-end electronics

The front-end electronics of the muon chambers is a BiCMOS custom VLSI chip made of a charge integrator and a settable threshold discriminator (MAD ASIC)[17]. Since the front-end circuit is a charge sensitive device, the SEE associated with it is the detection of energy deposition inside the integrated circuit simulating a pulse over threshold (SET).

Two prototypes were tested both on thermal and fast neutrons. Since access to the boards was easier, in the fast neutron tests we modified the threshold settings in order to verify that SEE cross section was depending on the actual threshold.

The average cross section per readout channel is reported in Figure 10 showing a roughly exponential behaviour as a function of the threshold. Also in this case the quoted SEE cross section assumes that only neutrons with energy above 3 MeV will induce a SEE. It is relevant to notice that in this case also there is a non-negligible contribution from thermal neutron interactions with the device. The predicted noise rate is of a few thousand spurious counts in 10 years of LHC activity, well below the expected noise contribution from the electronics itself and the connected detector channel.

Some test runs were performed with heavy ions (bromine, silver and iodine) showing the same threshold dependence of SEU events. No threshold dependence and one order of magnitude lower SET cross section was found after masking the input ASIC stage, showing that SETs are

mostly occurring in the charge preamplifier. Furthermore no test gave evidence of latch-up events, even at the large energy deposition associated with heavy ion interactions.

## 7. SEE on high voltage distribution system

The HV distribution system will be constructed using an A877 module being developed by CAEN. Prototypes of this module were tested for radiation sensitivity. A module consists of control and monitoring cards and HV distribution cards. A scheme of the HV channel regulator is shown in Figure 11a. The SEE sensitive part of the module is the power transistor. Several devices for this part of the circuit were tested:

- a VMOS (MTP-3N120)
- an IGBT (SKP02N120)
- a HV npn transistor (BUL216)

As an alternative scheme a high voltage channel regulator using a DC-DC voltage multiplier driven by LV MOSFET devices and a transformer able to operate in a magnetic field up to 0.2 T (Figure 11b) was also tested.

The VMOS device was tested under neutron irradiation (fluence equal to  $10^{12}$  cm<sup>-2</sup>), while the others were tested under proton irradiation (fluence below  $5 \times 10^{10}$  cm<sup>-2</sup>). The VMOS and the IGBT solutions could not stand even a low radiation dose, showing degradation after few minutes of irradiation. Indeed the tests done after irradiation showed single event gate ruptures (SEGR), since the gate was short-circuited to the channel in 20% of the cases. None of the devices survived the test and the leakage current (measured to be about 50 nA at 800 V before the test) increased by several orders of magnitude (to few tenths of  $\mu$ A) after irradiation. Instead the other alternatives were both working, although the BJT showed a considerable change in its characteristics: a correlated decrease by one order of magnitude in the collector currents and the  $h_{FE}$  parameters of the transistors measured after irradiation was found.

There were few cases of HV misreading in the module of the distribution system dedicated to the monitoring ( $\sigma_{SEU} = 3 \times 10^{-11}$  cm<sup>2</sup>), corrected by internal CPU refresh in a 10 seconds cycle.

## 9. Unclassified SEE

We recorded few cases of strange behaviour when performing the tests of the boards and devices, with the exception of the front-end electronics. We had system faults, I/O lines upsets, multiple upsets and communication loss. The probability of occurrence of these events was negligible. We believe that these events are not real SELs, but that they are rather associated to SEUs on either bus control and monitoring devices or clock distribution circuitry. Some cases were solved by triggering an automatic system reset, while in other cases a hardware reset was necessary. A small fraction of similar cases is probably unavoidable due to the complexity of the electronics system.

## 10. Conclusions

We found evidence of neutron induced SEE due to fast and thermal neutrons as well as protons. Evidence for an energy threshold around 3 MeV and energy rising SEU cross section for SRAMs is reported.

A rough scaling property was found that could be useful in order to predict overall device performance with respect to neutron irradiation, only through measurements with 60 MeV protons, as required by CMS validation policy.

We measured SEE cross sections or derived upper limits for all the important devices to be used in the muon barrel electronics. Although some system blocks were observed, no evident latch-up was observed, hence validating the architectures and the protection circuitry foreseen for the final boards layout.

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The development of HV system was carried on in the frame of a collaboration agreement between INFN and CAEN s.p.a. In particular G. Passuello participated in the test preparation, data acquisition and analysis on HV modules.

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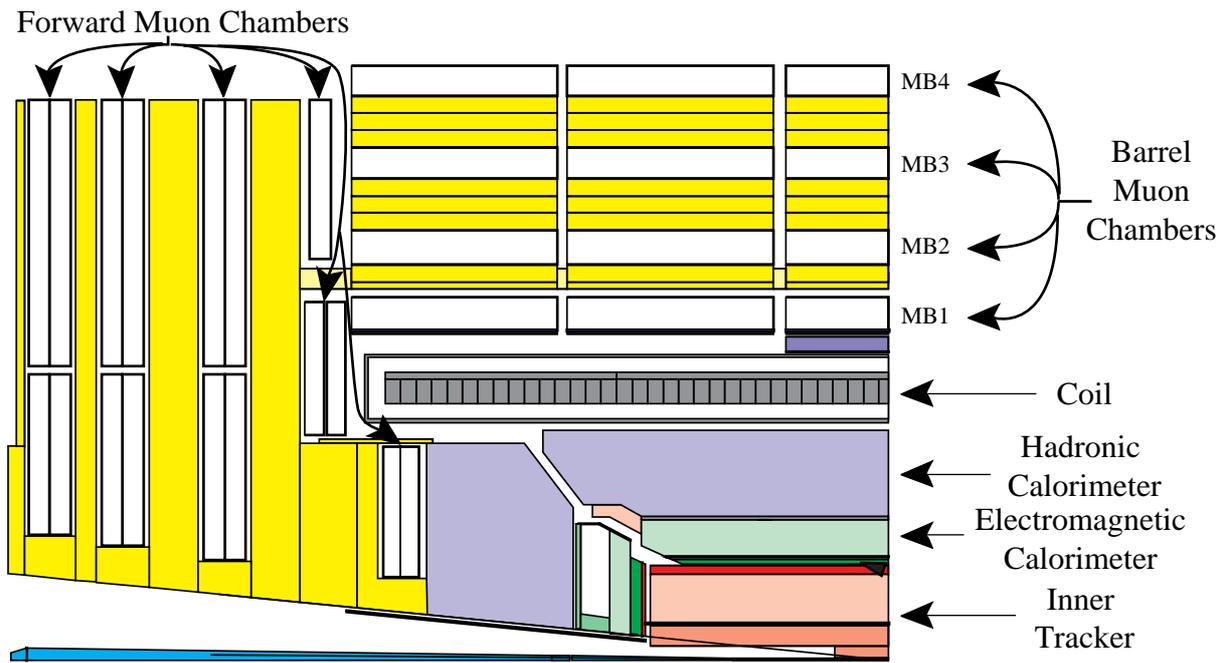
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## Figure captions

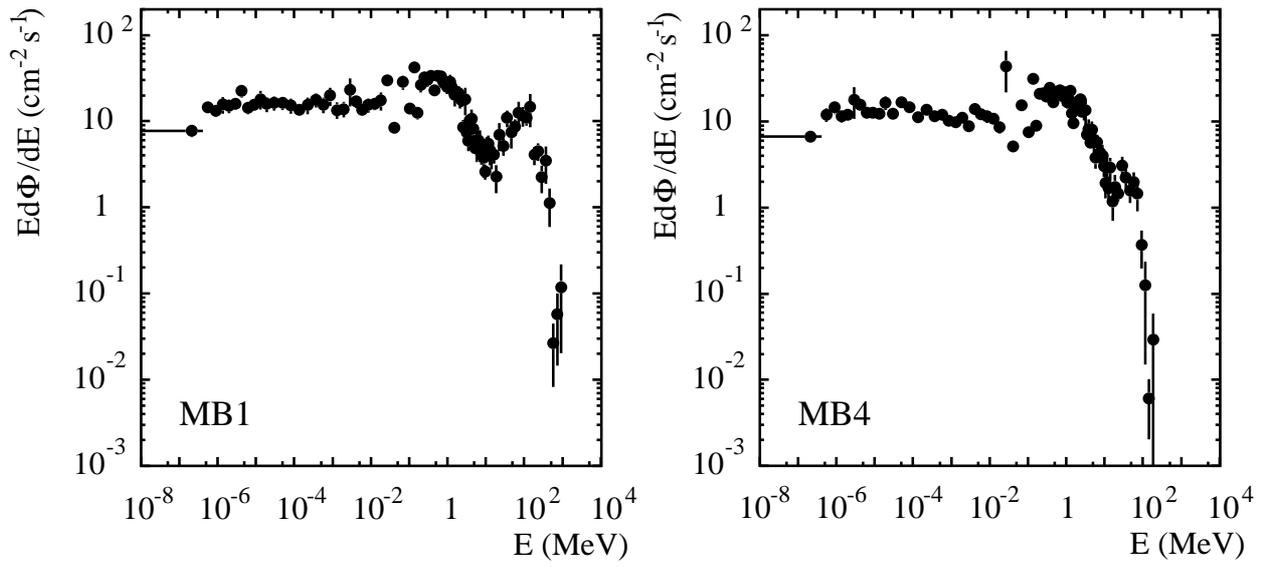
- Figure 1** - Longitudinal cut of CMS detector showing barrel muon chamber locations and acronyms.
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- Figure 3** - Total non-elastic cross section for neutron and proton interactions on silicon.
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- Figure 11** - Scheme of anode HV channel regulator of A877 module. Figure (a) shows the MOS solution and Figure (b) shows the DC-DC solution. IGBT and BJT solutions are similar to MOS solution with appropriate transistor bias.

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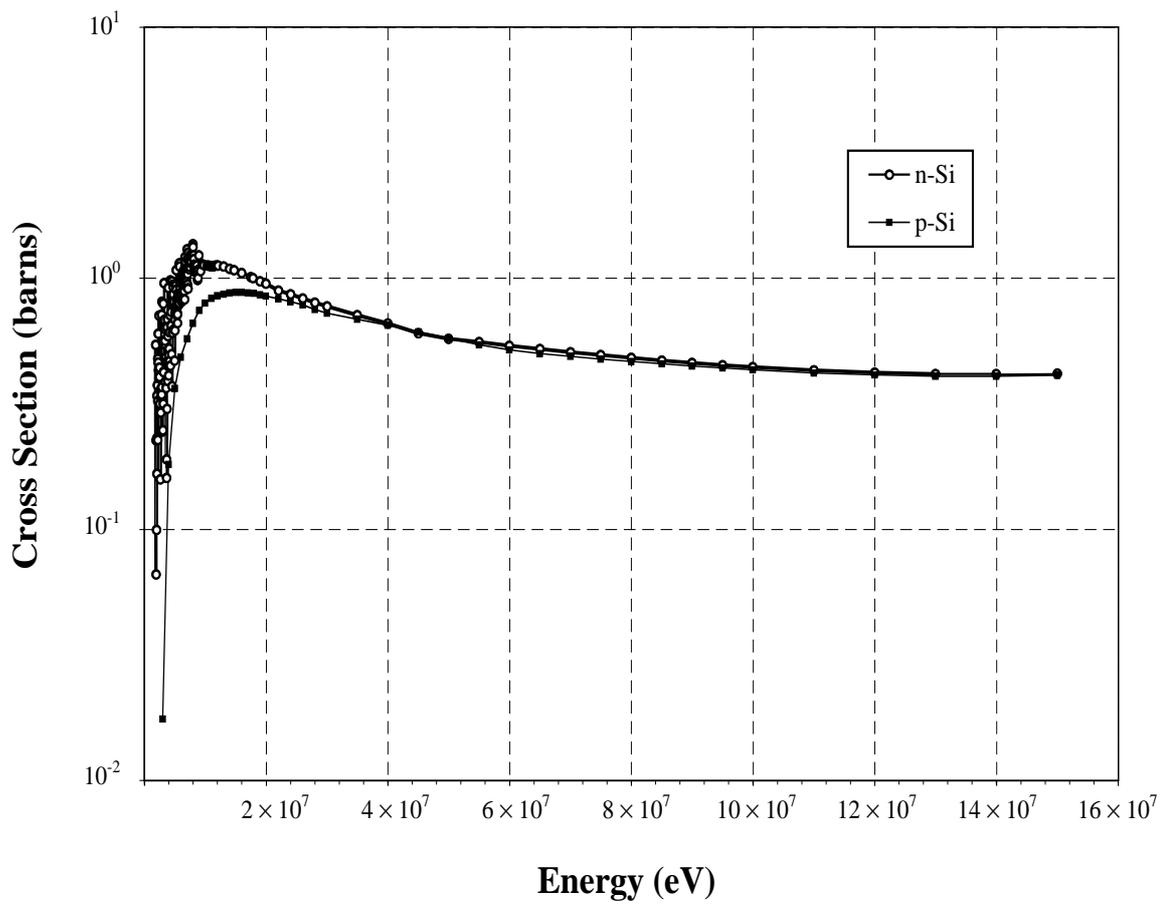
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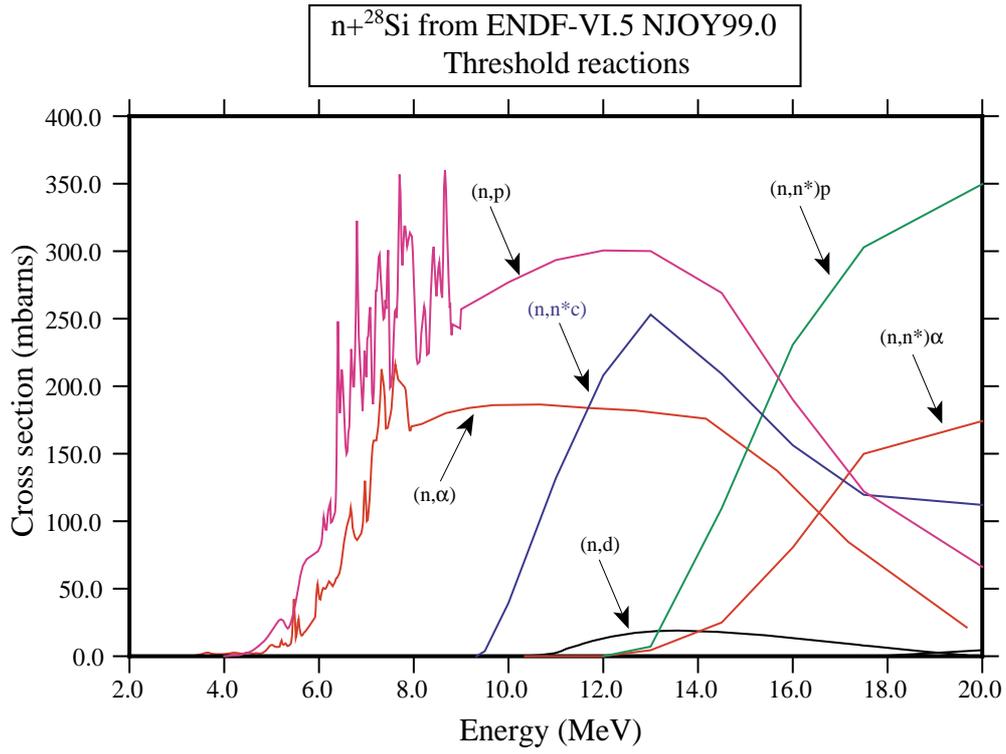
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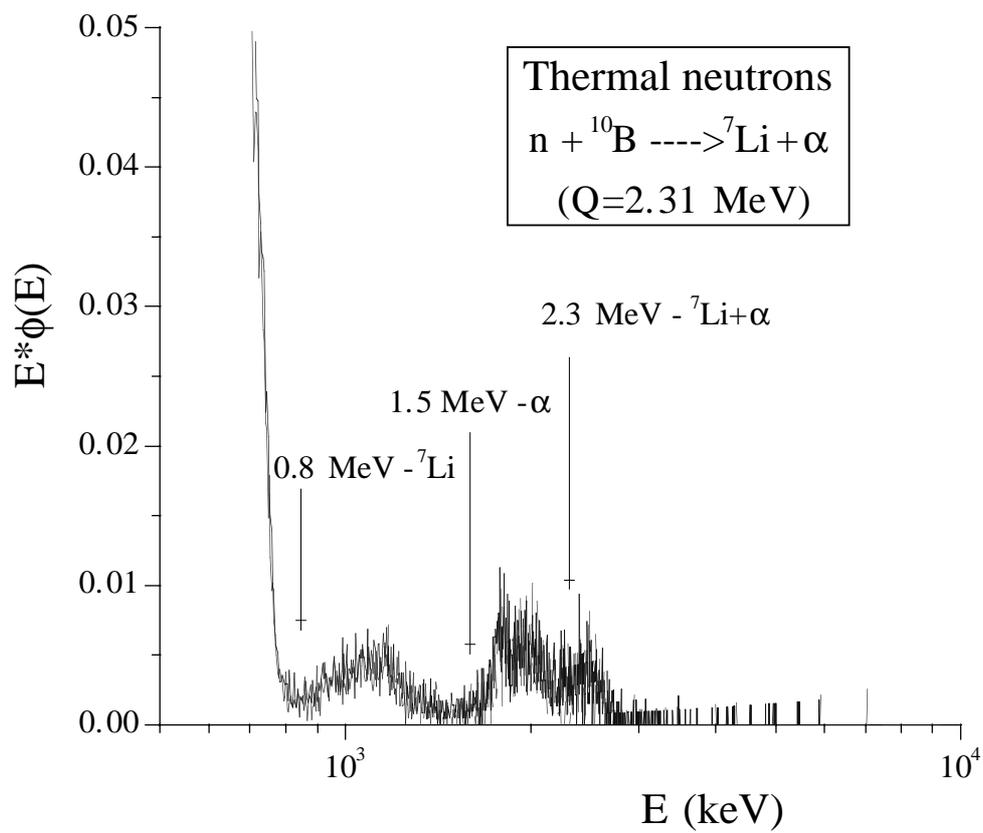
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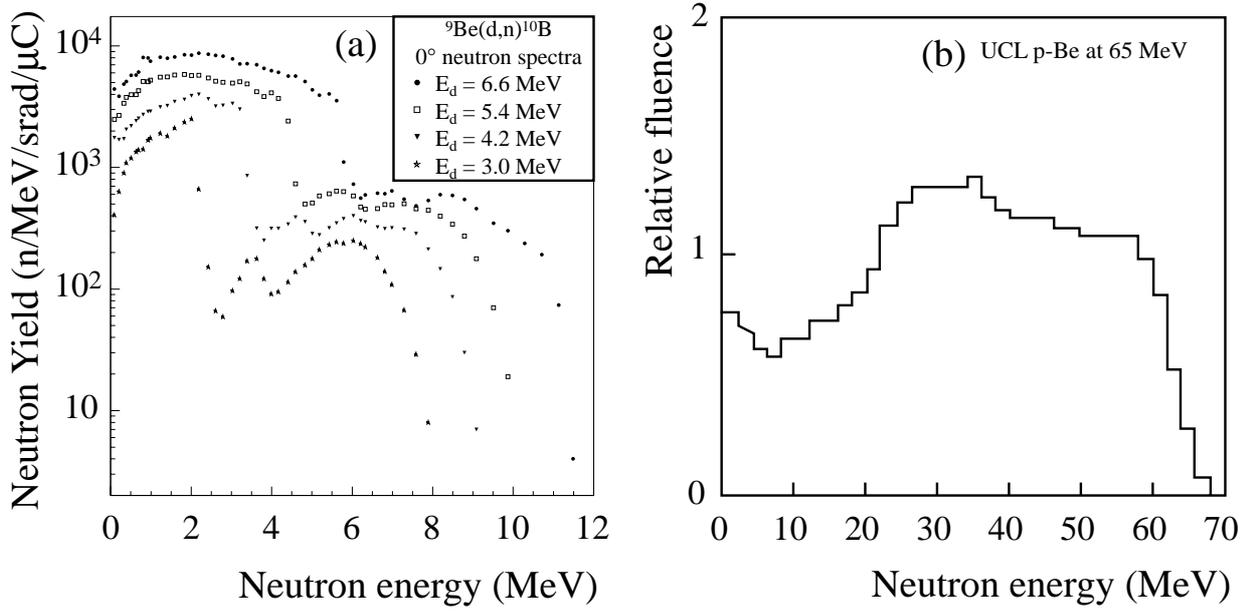
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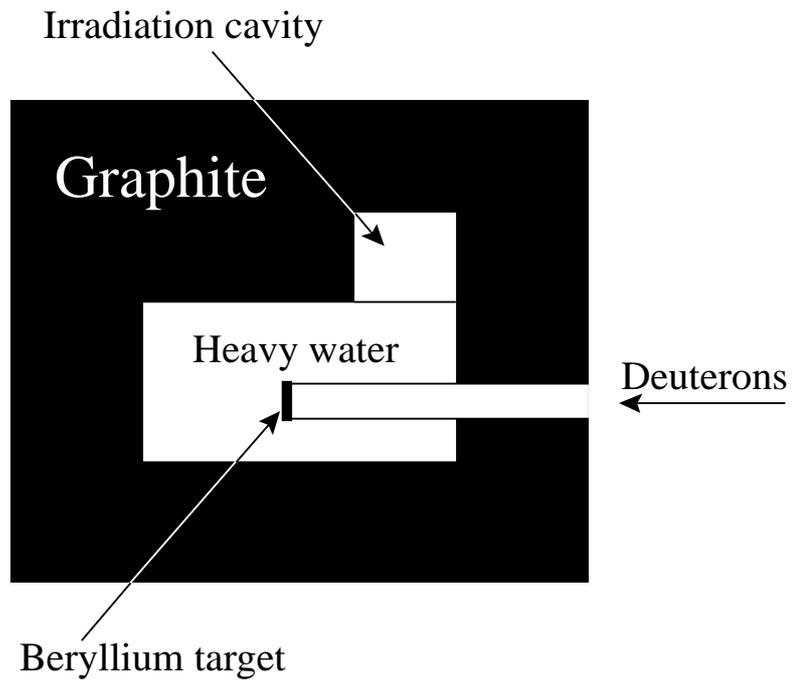
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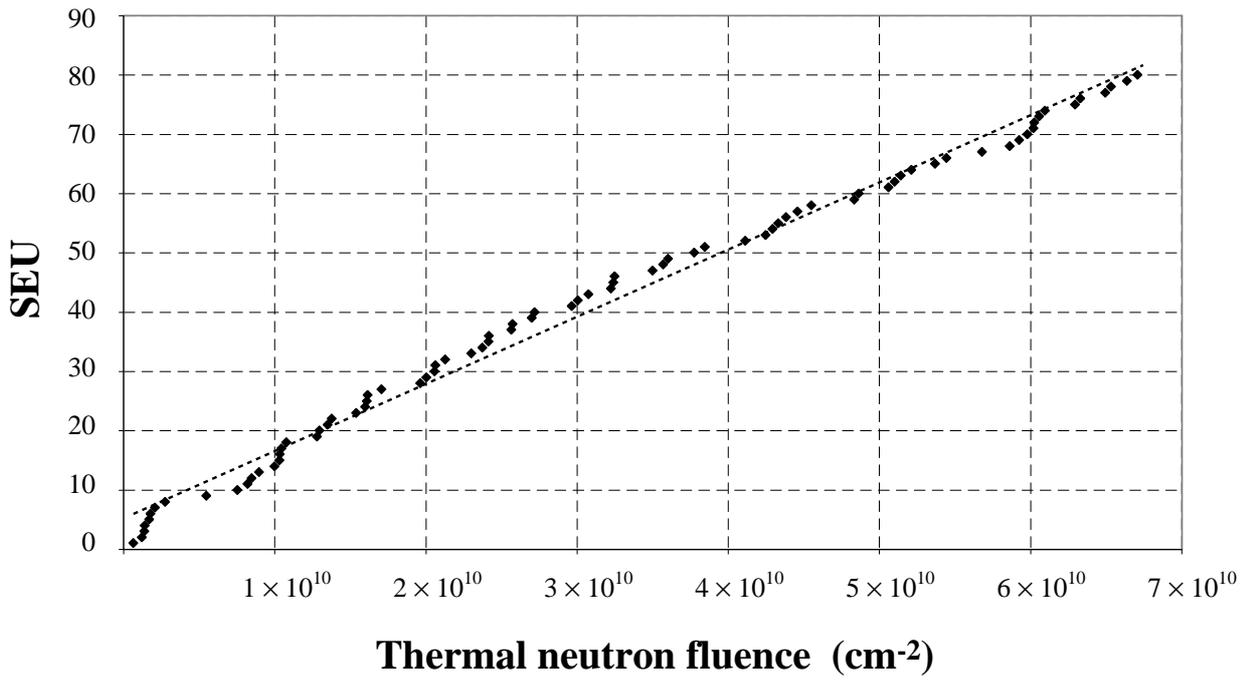
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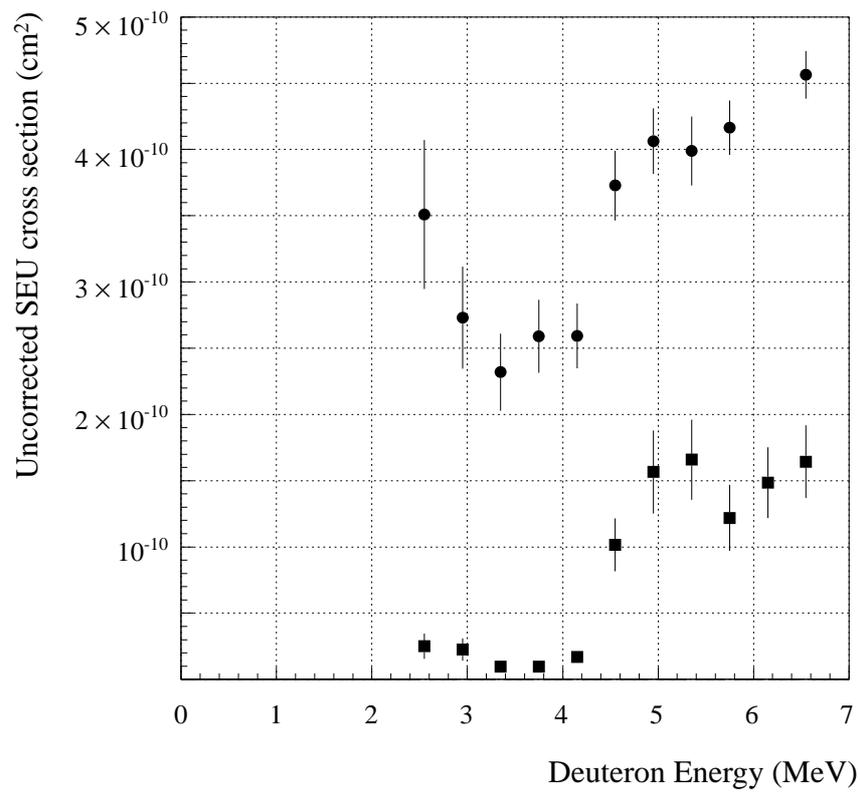
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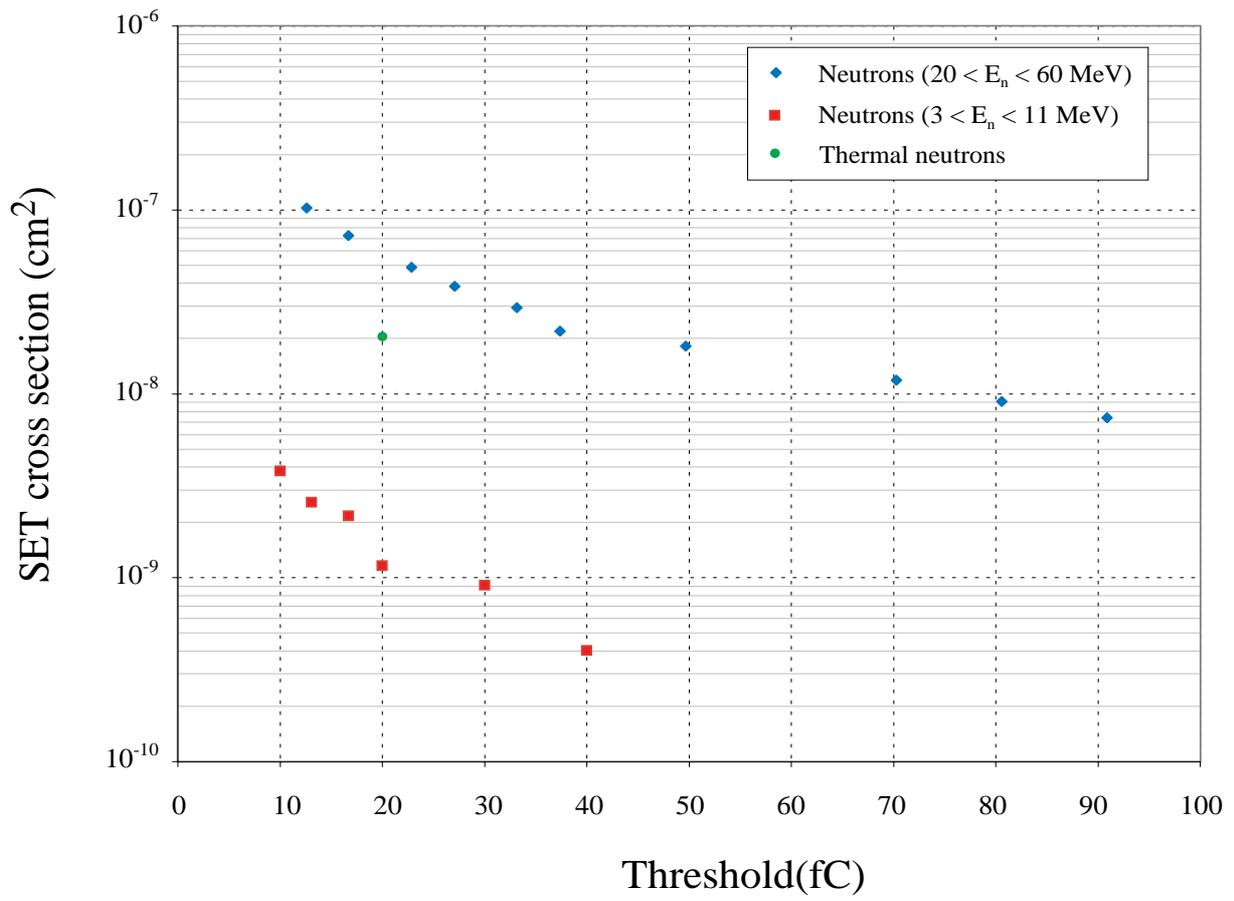
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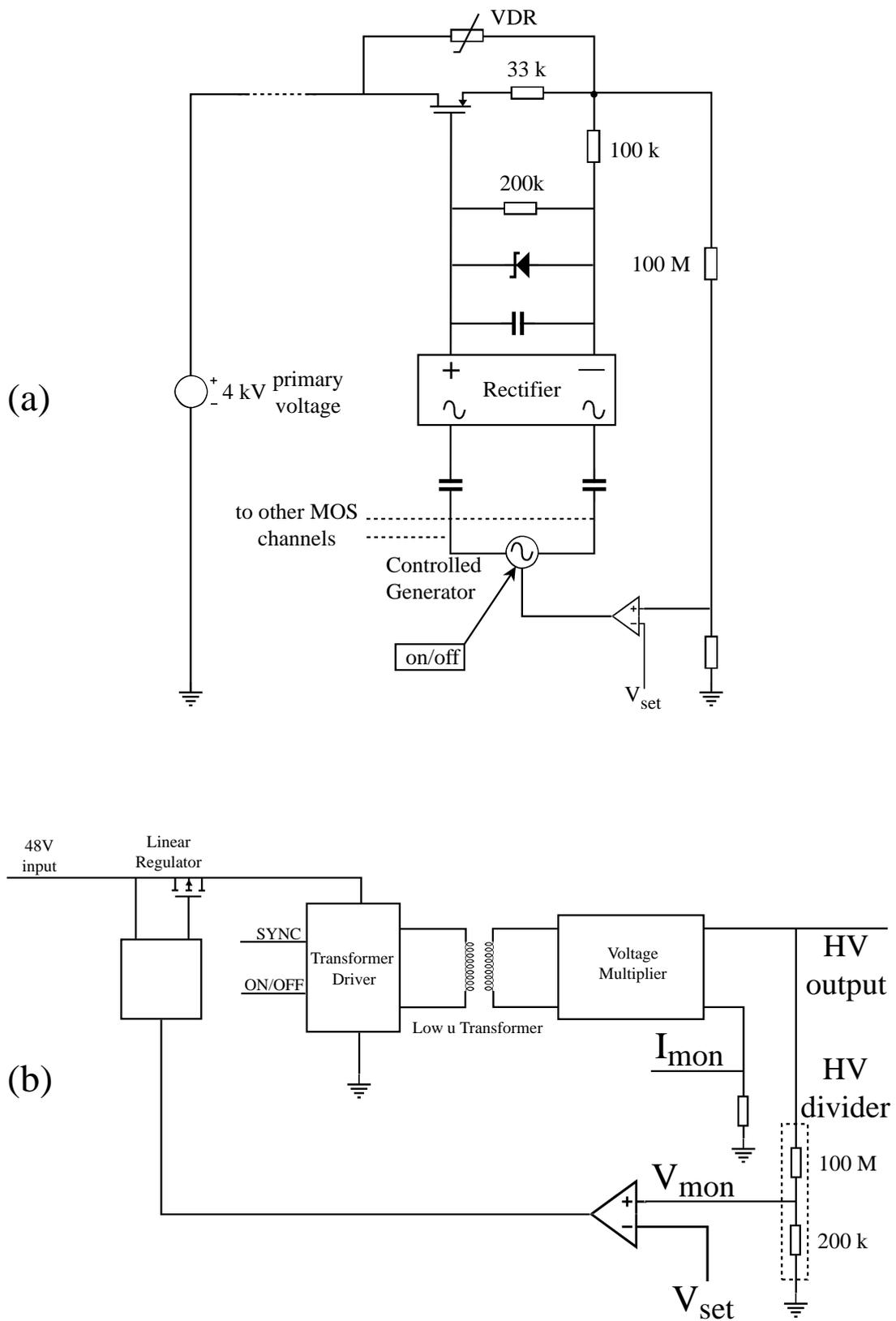
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**Figure 10-** Single Event Transients cross section on front-end circuit as a function of threshold for different neutron energy ranges. The expected working threshold is the lowest one.



**Figure 11-** Scheme of anode HV channel regulator of A877 module. Figure (a) shows the MOS solution and Figure (b) shows the DC-DC solution. IGBT and BJT solutions are similar to MOS solution with appropriate transistor bias.

	Neutron flux ( $\text{cm}^{-2} \text{s}^{-1}$ )				Charged hadron flux ( $\text{cm}^{-2} \text{s}^{-1}$ )	Dose (10 years LHC activity) (Gy)
	Total	E > 0.1 MeV	E > 3 MeV	E > 20 MeV		
MB1	458	128	33	23	1.6	0.2
MB2	153	61	-	4	0.5	0.02
MB3	50	10	-	0.3	0.005	0.006
MB4	584	126	20	7	0.02	0.06
CAVERN	784	179	-	18	0.2	0.4

**Table 1-** Expected average ionizing particle flux in the locations of muon barrel electronics [2].

Reaction Products	Q-Value (MeV)	Threshold (MeV)
$^{29}\text{Si} + \gamma$	8.47362	0.00000
$^{28}\text{Si} + n$	0.00000	0.00000
$^{25}\text{Mg} + \alpha$	-2.65368	2.74935
$^{28}\text{Al} + p$	-3.85991	3.99908
$^{27}\text{Al} + d$	-9.36044	9.69791
$^{24}\text{Mg} + n + \alpha$	-9.98440	10.34438
$^{27}\text{Al} + n + p$	-11.58503	12.00271
$^{26}\text{Mg} + ^3\text{He}$	-12.13830	12.57592
$^{21}\text{Ne} + 2 \alpha$	-12.53967	12.99177
$^{27}\text{Mg} + 2 p$	-13.41301	13.89660

**Table 2-** Available channels for the  $n+^{28}\text{Si}$  interaction below 20 MeV neutron energy [7].

Device	Producter	Type	Memory size(kbytes)
SRAM	SONY	CXK581000AM-70LL	128
SRAM	TOSHIBA	TC554161AFT-70L	512
Microprocessor	MOTOROLA	MC68HC16	1
EPROM	ATMEL	AT27C512R-15JC	64
FLASH	ATMEL	AT29C010A-12PC	128
BTI ASIC	ES2	0.5 $\mu$ m LTCC substrate	< 1
TRACO ASIC	ATMEL	0.5 $\mu$ m in dies	3
TSS ASIC	ALCATEL	0.5 $\mu$ m in dies	< 1
FPGA	ACTEL	A54SX32-3PQFP208	
FPGA	ALTERA	EPM7128STC100-10	

**Table 3-** List of tested memory devices. BTI (Bunch and Track Identifier), TRACO (Track Correlator) and TSS (Track Sorter Slave) are custom integrated circuits designed for the muon trigger.

	SEU cross section per device (cm <sup>2</sup> )	
	Neutrons ( $3 < E_n < 11$ MeV)	Neutrons ( $20 < E_n < 60$ MeV)
SONY #1	$(0.94 \pm 0.08) \times 10^{-9}$	$(1.03 \pm 0.08) \times 10^{-8}$
SONY #2	$(5.73 \pm 2.86) \times 10^{-12}$	$(8.99 \pm 2.42) \times 10^{-10}$
SONY #3	$(0.84 \pm 0.19) \times 10^{-12}$	—
SONY #4	$(5.90 \pm 4.15) \times 10^{-12}$	—
SONY #5	—	$(1.50 \pm 0.14) \times 10^{-10}$
SONY #6	—	$(1.70 \pm 0.15) \times 10^{-10}$
TOSHIBA #1	$(1.24 \pm 0.04) \times 10^{-9}$	—
TOSHIBA #2	$(1.46 \pm 0.05) \times 10^{-9}$	—
TOSHIBA #3	$(0.95 \pm 0.03) \times 10^{-9}$	—
TOSHIBA #4	$(2.05 \pm 0.07) \times 10^{-9}$	—
TOSHIBA #5	$(1.46 \pm 0.05) \times 10^{-9}$	—
TOSHIBA #6	$(1.03 \pm 0.03) \times 10^{-9}$	—

**Table 4-** SEU cross section for several devices of the same type in different test conditions.

	Thermal neutrons	Neutrons $3 < E_n < 11 \text{ MeV}$	Neutrons $20 < E_n < 60 \text{ MeV}$	Protons $E_p = 60 \text{ MeV}$
SONY # 1	$(1.13 \pm 0.20) \times 10^{-9}$	$(0.94 \pm 0.08) \times 10^{-9}$	$(1.03 \pm 0.08) \times 10^{-8}$	-
SONY # 2	$< 1.38 \times 10^{-10}$	$(0.57 \pm 0.29) \times 10^{-11}$	$(8.99 \pm 2.42) \times 10^{-11}$	-
TOSHIBA	$(4.71 \pm 0.54) \times 10^{-8}$	$(1.69 \pm 0.05) \times 10^{-9}$	-	$(1.86 \pm 0.02) \times 10^{-8}$

**Table 5-** SEU cross sections for the same device due different incident particles.

Device	SEU cross section per device (cm <sup>2</sup> )	SEU cross section per bit (cm <sup>2</sup> )
SONY SRAM	$(1.03 \pm 0.08) \times 10^{-8}$	$(2.46 \pm 0.08) \times 10^{-15}$
TOSHIBA SRAM*	$(1.86 \pm 0.02) \times 10^{-8}$	$(1.77 \pm 0.07) \times 10^{-14}$
MICROPROCESSOR	$(4.90 \pm 0.02) \times 10^{-11}$	$(5.98 \pm 0.99) \times 10^{-15}$
TRACO ASIC*	$(5.25 \pm 0.51) \times 10^{-10}$	$(2.14 \pm 0.21) \times 10^{-14}$
TSS ASIC*	$(4.67 \pm 1.91) \times 10^{-12}$	$(8.40 \pm 3.43) \times 10^{-15}$
BTI ASIC	$< 9.51 \times 10^{-12}$	$< 3.37 \times 10^{-14}$
FLASH	$< 9.51 \times 10^{-12}$	$< 9.07 \times 10^{-18}$
EPROM	$< 9.51 \times 10^{-12}$	$< 1.81 \times 10^{-17}$
ALTERA FPGA*	$< 4.75 \times 10^{-11}$	—
ACTEL FPGA*	$< 2.90 \times 10^{-12}$	—

**Table 6-** SEU cross section for all tested memory devices. The lower limits are 90% confidence level quotations. Items marked with (\*) refer to measurements with protons at 60 MeV, while the other measurements were done with neutrons of energy between 20 and 60 MeV.