Efficiency Studies of the Front-end Trigger Device of the Muon Drift Tubes for the CMS detector at LHC

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Abstract

Three simplified prototypes of the first level trigger front-end device for the muon barrel drift chambers of CMS were tested on a chamber prototype. Tests were performed at several incidence angles of a muon beam and with different magnetic field configurations.

The recorded drift-times were also used to test a full software model reproducing the actual algorithm applied in the final ASIC being produced.

The efficiency performance of this software model and of the tested prototype are presented in this paper.

1. Introduction

Any first level muon trigger system for a detector at the LHC accelerator must meet its requirements in terms of timing and rates. The time resolution should be well below the 25 ns time between successive bunch crossings to reduce the event size and the space resolution should provide the best possible p_T assignment of the trigger candidate track to allow an effective muon momentum cut.

In the CMS [1] experiment a fully dedicated muon trigger detector, made of Resistive Plate Counters, is complemented and integrated by a more sophisticated trigger based on the tracking chambers (drift tubes in the barrel region and proportional chambers with cathode readout in the forward region).

The proposed muon chambers trigger baseline consists of a multistage scheme, where the front-end trigger device is the most demanding stage, since it is supposed to be able to make a rough local track segment reconstruction and to uniquely identify the parent bunch crossing of the track candidate. The triggering front-end device being developed for the muon barrel chambers is called Bunch and Track Identifier (BTI). The other devices deal with the association of segments of tracks in different chambers and p_T assignment.

A barrel chamber prototype was tested in the CERN H2 muon beam in 1995 and 1996. The chamber was equipped with three prototypes of a simplified version of the BTI. The results of the tests as well as the performance of the software model of the full scale device applied to the recorded drift time data, are summarized in this paper.

2. Test Setup

The test was performed in the CERN H2 muon beam where the drift chamber prototype was put on a rotating support inside the gap of a magnet.

The chamber prototype consists of four layers of 16 drift tubes each. The layers are staggered by half a tube.

The drift cell has a cross section of 39x11 mm^2 and the drift field is optimized for linearity of the space-time relationship by means of two C-shaped cathodes and two shaping electrodes facing the wire.

The results on the performance of the chamber are presented elsewhere[2]: we only stress that the trigger performance is largely connected to the drift cell design.

The chamber prototype was equipped with three BTI prototypes, realized with Field Programmable Gate Arrays (FPGA), operated with a free running 40 MHz clock. The BTI is a synchronous device and therefore its performance is strictly related to the phase of the clock with respect to the particle crossing time. In any collider the synchronization between the clock and the interaction time is assured from the pulsed nature of the beam collisions, while it is random in any standard fixed target test where the beam is a continuous stream of particles. Therefore, along with the drift times and the trigger signals generated from the BTI prototype, also the BTI clock was recorded to allow the computation of its phase with respect to the test beam trigger.

The data were recorded using 2277 Lecroy TDCs, with 1 ns least count and multihit capability. The cards carrying the FPGA device were put after 60 m long cables: the delay difference between signals on different wires caused by the line length was

measured with test pulses and was within ±4 ns from the average value. No adjustable delay was used in the setup in order to achieve cable's length equalization.

All the data used in the analysis described in the following pages were taken with voltages V_{anode} = 3600V, $V_{cathode}$ = -1800V and $V_{electrode}$ = 1800V and with the discriminator threshold set to 4 fC.

Data were taken for nominal inclinations of the beam with respect to the normal to the chamber ranging from $\psi = 0^0$ to $\psi = 49^0$ and for several values of the magnetic field

3. Description of the Bunch and Track Identifier

In this section we will give a description of the working principle of the BTI and a brief description of its implementation in the custom integrated circuit being developed now and in the FPGA device already tested.

Although developed starting from the same idea, the two devices have some important differences that will be pointed out and discussed.

3.1 Working Principle

The Bunch and Track Identifier was studied to work on groups of four layers of staggered drift tubes called Superlayers, aiming to the identification of the tracks giving signals in at least three of the planes.

In this way if the drift time of a tube is missing, due to inefficiency, or wrong, due to the emission of a δ-ray, the identification is still possible, since there are still three useful cells giving the minimum requested information. It is also insensitive to all uncorrelated single hits.

The algorithm used in the device is a generalization of the mean-timer method[3].

The digitized signals of the wires can be fed in shift registers of depth equal to the maximum drift time T_{MAX} and shifted, in the same direction of the electron drift in the corresponding cell, at bunch crossing frequency.

After the fixed time interval T_{MAX} from the muon crossing time, the hits will be aligned in the shift registers as shown in Fig. 1, allowing the identification of the interaction originating the muon.

Furthermore the position of the hits inside the shift registers will form an image of the muon track, thus allowing the extraction of the full track information: the track impact position and the track direction can infact be calculated from the shift times $t_s = T_{MAX} - t_d$.

3.2 Design of the BTI ASIC

Each BTI is connected to nine wires allocated as shown in Fig. 2. Each Superlayer is equipped with one BTI every four wires and therefore the BTIs are overlapped by five wires This overlap assures a good redundancy and that every track, with angle within the maximum acceptance range, is fully contained in at least one BTI.

The actually evaluated parameters are the position, computed in the Superlayer centre, and the angular k-parameter $k = h \tan \psi$, with ψ being the angle of the track with respect to the normal to the chamber plane in the transverse projection and $h = 13mm$ being the distance between the wire planes.

Position and angular resolution depend on the drift velocity and on the sampling frequency of the device. The drift velocity without magnetic field and for the gas mixture used in the prototype (Ar/CO_2 85/15) is 57 μm/ns and the foreseen sampling frequency is 80MHz. In these conditions the angle is measured with a resolution better than 60mrad and the position is measured with a resolution of 1.4mm.

The BTI trigger requires that the hits belonging to the track are aligned within a programmable tolerance and that the track k-parameter is within the programmed angular acceptance. With the present geometric parameters of the chamber the BTI is fully efficient up to $\psi_{MAX} = \pm 45°$.

The track information is accompanied by a TRG signal and is transmitted with a fixed delay of T_{MAX} plus 4 clock cycles needed for the input signal synchronization and for the BTI calculations.

The actual BTI candidate track finding algorithm computes in parallel several track patterns hypotheses: a pattern is identified from a sequence of wire numbers and labels stating if the track crosses the tube on the right or on the left of the given wire (e.g. in Fig. 2 the track corresponds to the pattern 5L3R6L4R). Any given pattern includes six couples of planes (AB, BC, CD, AC, BD, AD), each one providing a measurement of the position (through an *x-equation*) and of the k-parameter (through a *k-equation*) of the track.

The value of a *k-equation* is proportional to the distance between the hits of a couple inside the shift register at any clock cycle and corresponds to a rough measurement of the track direction at that cycle. Since the hits are shifted inside the register, this value is time dependent. Therefore each couple included in a pattern gives its own measurement of the track direction: the hits are aligned when, after applying the couple dependent proportional factor, the values of the k-parameter of each couple are equal.

Hence at every clock cycle all *k-equations* are computed and a BTI trigger is generated if at least three of the six k-parameters associated to any of the patterns are in coincidence. The tolerance on the coincidence of the *k-equations* is defined according to the resolution of each couple that in turn depends on the distance between the wires and was chosen to allow a maximum cell linearity error equivalent to 25ns. This coincidence allows the bunch crossing identification owing to the time-dependence of the *k-equations* value.

If there is a coincidence of all the six k-parameters, the trigger corresponds to the alignment of four hits and it is marked as High Quality Trigger (HTRG), while in any other case, with a minimum of three coincident k-parameter, it is due to the alignment of only three hits and it is marked Low Quality Trigger (LTRG). The angular resolution of LTRGs is track pattern dependent and is generally worse than the one of HTRGs.

If several track patterns give a response, the HTRG is chosen as the triggering track pattern. If there is more than one HTRG or the triggers are all LTRGs, the first one, in an arbitrarily defined order, is selected.

The request of the alignment of any three hits is a substantial source of background, since it introduces two effects creating false triggers.

There is a large probability that the alignment of four hits at some clock step produces the alignment of just three of them at the step just before or after the HTRG signal, thus generating “ghost” LTRG candidate tracks.

There is also some probability that a random LTRG could happen at any clock step with some fancy k-parameter due to the left-right ambiguity, that is duplicating the possible choices for every hit.

The noise reduction of the former kind of “ghosts” is obtained issuing the LTRG signal only if at the neighbouring steps there is no HTRG generated: this mechanism is called Low Trigger Suppression (LTS). The noise reduction of the latter kind of “ghosts” is obtained by acting on tolerances in the association phase of the next stages of the trigger.

The impact position of the muon is not entering the track selection algorithm and it is computed only for the selected triggering pattern.

K-parameter and position of the track, as measured from the corresponding equations, coded in 6 bits, and one trigger quality bit, marking HTRGs, are transmitted on the BTI track_data bus.

A complete software model of the device was developed and interfaced to the full simulation of the CMS detector. Results of the simulation and details on the devices following the BTI in the trigger chain can be found in [4].

3.3 Design of the BTI Prototype

While developing the design of a dedicated ASIC, we produced a simplified version of the device using FPGA technology.

Such a prototype is obviously limited by the size and speed of the integrated circuits available on the market. The implementation of the algorithm encountered serious space limitations, forcing us to downgrade the requirements.

The actual gate array used was XILINX XC4013, 6 ns grade.

The number of wires allocated to the prototype is eight and only a subgroup of relevant couples of wires is considered.

As shown in Fig. 3, the signals coming from each couple of wires are shifted in opposite directions inside a pair of shift registers whose depth is programmable as a function of the maximum drift time. The shifting frequency is 40 MHz compared to 80 MHz of the final VLSI circuit.

At every clock step the AND of the two vertically aligned bits of the shift registers is evaluated. The tolerance allowed in the AND evaluation is built-in from the fact that the signal running in the upper shift register is two cells wide, while the signal inside the lower one is only one cell wide. Simulations proved that this choice was minimizing the number of false triggers due to random alignments of the signals, while assuring a good efficiency.

There is no calculation involved in the explained scheme, since the beam incidence angle is always known in test beam setup and the BTI prototype was designed as a device programmable for fixed incidence angle.

Infact each wire couple should give a coincidence when the distance between the signals inside the shift registers is corresponding to a chosen angle. In order to achieve the coincidence for vertically aligned bits the signals are therefore input to a programmed depth inside the upper shift register. The input position is determined for every programmed angular range to assure the coincidence at a defined time. In this way the couples give the coincidence only for tracks with the programmed direction, but their output signals will not be anymore synchronized, because the input position is couple dependent. Therefore a look-up table, including an initial shift and an output predefined delay chosen to synchronize each couple, was loaded for each angular configuration.

The couples are grouped in patterns, each one including 3 or 4 couples, whose coincidence is evaluated at every clock cycle. Since the couples can give a signal only

for the programmed track direction range, the request on the coincidence in the patterns can be relaxed with respect to the full design. Therefore a Low Level Trigger (LTRG) is generated if any two of the couples of the pattern give a coincidence signal, while a High Level Trigger (HTRG) is generated if all the couples of the pattern are available. The information about the triggering pattern and the trigger type is not recorded. A LTS suppression mechanism was included also for the FPGA prototype: a LTRG is issued only if there is no HTRG at the neighbouring clock steps.

The algorithm needed to calculate the position of the trigger candidate track could not be implemented, due to the limited space available inside the chip.

The BTI prototype was programmed for a maximum drift-time T_{MAX} = 350 ns. This programmation was never changed, even when the magnetic field was switched on modifying the apparent drift velocity.

A more detailed description is available in [5].

4. Results

The major task of the test was the evaluation of the efficiency of the triggering mechanism, being all the other interesting checks ruled out from space limitations in the FPGA implementation of the BTI.

The efficiency is defined as the fraction of events giving a BTI trigger at the expected time (equal to T_{MAX} plus the time necessary for the BTI internal calculations) with respect to the particle crossing time given by the experiment trigger.

In the following sections we will describe the performance of the BTI prototype and the same studies done on the BTI software model.

4.1 Efficiency versus Synchronization

The FPGA clock cannot be synchronized with the random time of passage of the muons during the spill time. Therefore the first important check was the performance of the BTI prototype as a function of the phase of its clock with respect to particle crossing, since we expect that events are assigned the wrong crossing when the clock and the interacting particles are outphased.

The efficiency of the device as a function of the clock phase is shown in Fig. 4 for a sample of data at $\theta = 0^0$ and B = 0T. The efficiency exhibits an almost flat top about 10 ns wide around the central value and drops when the BTI clock is too early or too late. A more detailed analysis of the data shows that the missing fraction of events is assigned to the step before the expected one if the clock is too early and to the step after the expected one if the clock is too late.

The event sample considered in the analysis of the BTI prototype was therefore restricted to the events where the recorded time phase was within ±4 ns from the phase of maximum efficiency.

This limitation does not apply to the computations done using the BTI model, since the computation is done offline using the recorded TDC data: all the recorded events can be used since their reference time is the experiment trigger.

As in the case of the FPGA prototype the full scale device is supposed to have registers of programmable depth, set as a function of the actual drift velocity and therefore it needs to be synchronized to correctly identify the parent interaction.

The full scale BTI setup procedure is controlled by two parameters: the first one determines the depth of the shift register, using the measured maximum drift time T_{MAX}, and the second one provides a fine tuning of the device by means of a programmable delay common to all the wires' inputs. The combined action of these two parameters can be interpreted as a time setting.

We computed the rate of triggers at the expected step for a fixed sample of events, modifying the input parameters. We have observed that the result of the setup procedure slightly depends on the actual track inclination, due to the drift velocity dependence on the incidence angle. We therefore averaged the rate value for all beam directions at B=0T.

The average rate curve of this fine tuning as a function of the parameters settings is shown in Fig. 5 and looks quite similar to the performance as a function of the clock phase obtained on the test beam for the FPGA device (see Fig. 4). This curve is less sharp, since there is no angular acceptance cut in the BTI model. The chosen setup was the one giving the highest rate of triggers and, as in the case of the FPGA prototype, it was never changed.

This analysis points out that the performance at LHC will largely depend on a good synchronization scheme. The best setup procedure to assure this synchronization is still under study.

4.2 Efficiency versus Track Direction

The angular acceptance of each pattern programmed in the FPGA prototype depends strongly on the couples included in the pattern. Therefore the actual beam incidence angle was rather critical for the performance of the device. The beam divergence is about two degrees, but the angular acceptance is shrinks when ψ increases, becoming half a degree at $\psi = 30°$. For a good definition of the data sample it was therefore necessary to determine the actual direction of the incident muon to set a cut on the incidence angle.

Since an external reference is missing, the track parameters can be computed using the drift times associated to an event fitting a straight line through the four layers. We reconstructed all the tracks with at least 3 points using a fit probability cut at 0.1% and allowing the rejection of the worst measurement for the 4-point tracks.

The request of a fitted track reduces the sample size and excludes two contributions to the overall inefficiency. The first contribution is chamber geometrical acceptance, since it excludes the events in which the fit could not be performed due to two missing drift times, and the second contribution is the generation of penetrating δ-rays or electromagnetic showers that spoiled the drift time measurement in more than one cell.

It is interesting to avoid the inclusion of the geometrical chamber acceptance in the efficiency calculations, since we are only interested in the device performance. Instead the contribution of showers depends only on the amount of material in front of the chamber: this material was negligible and therefore it is expected to be around 0.6%, looking at previous measurements[6]. Therefore the quoted efficiency includes only the effect of soft δ-rays fully contained in a cell (about 5% per cell).

The angular limitation is not present in the model, since it is designed to be wide open in angle, therefore the only cut applied was the request of at least three hits in a BTI to avoid the inclusion of the geometrical efficiency.

As previously discussed the algorithm is generating noisy LTRG triggers: a typical time spectrum of the trigger signals is shown in Fig. 6. We notice that while the HTRG

signal is essentially clean, the LTRGs are dispersed in a wide temporal range around the expected step.

A LTS mechanism was designed to reduce the amount of false triggers. This mechanism is embedded in the FPGA prototype, while it can be switched off in the model. The results of the behaviour of the FPGA prototype and the designed full scale device (the latter with and without the LTS mechanism activated) are shown in Fig. 7.

The BTI model is expected to have larger efficiencies than those ones quoted for the FPGA prototype, since there is no angular acceptance cut in its design.

The LTS mechanism has a small impact (below 1% efficiency loss) up to $\psi = 34°$ and it is not anymore negligible at larger angles. This loss is related to the existing non linearity of the cell for these directions, that exceeds the internal tolerance. But on the other hand the use of the LTS mechanisms causes a factor 2 noise reduction.

4.3 Efficiency in Magnetic Field

Data were taken in magnetic field in several configurations. Unfortunately for most of these configurations the BTI prototype data were not available due to system faults, but the drift-times were correctly recorded and therefore the analysis of the trigger performance using the full scale BTI model could be successfully performed. Then in this section we will only quote the results of the software model.

The magnetic field components are defined in Fig. 8 with respect to the chamber layout: B_n is the component perpendicular to the chamber, B_w is the component parallel to the wires and B_v is the component parallel to the electric field (parallel to the drift velocity in absence of magnetic field).

The global effect of a magnetic field is an elongation of the electron drift path to the anode, resulting in a longer maximum drift time. It also introduces deviations from linearity of the space-time relationship, that are quite important for $B_w \neq 0$.

Data were taken with the chamber normal to the beam for several values of B_n or B_w or B_v separately, keeping null the other field components.

When the chamber was inclined in the magnetic field the situation was more complex: in the case of vertical wires the magnetic field had the two components $B_w = B\sin\psi$ and $B_n = B\cos\psi$, while in the case of horizontal wires the two components were $B_v = B\sin\psi$ and $B_n = B\cos\psi$.

The trigger efficiencies for the situation $B_w \neq 0$, $B_v = B_n = 0$ are shown in Fig. 9 for several track inclinations.

The efficiency shows a marked dependence on the field sign for inclined muons. This effect is explained from the drift lines distortion introduced by the magnetic field. The major effect is the tilting of the drift lines by the Lorentz angle in such a way that they do not appear anymore normal to the beam at $\psi = 0°$. Therefore the beam inclination with respect to the drift lines for one field sign approaches the normal and for the other sign is larger than the chamber nominal inclination. Of course the other sign of the chamber angle with respect to the muon beam direction should cause the symmetric behaviour.

The efficiencies measured for the other magnetic field configurations are reported in Table 1, where for the inclined beam situations the data where grouped to compare conditions with B_n almost constant.

In CMS the BTI is expected to work on chambers in which the field will be generally well below 0.2T. Only at some corner chambers the field is expected to be

highly inhomogenous with components B_n varying from 0T to 0.8T and B_w or B_v varying from 0T to 0.3T.

Looking at the obtained results we see that the effect is negligible for a field with components $B_n < 0.5$T and B_w or $B_v < 0.2$ T. The CMS region where the magnetic field exceeds these values is only the far corner of the first muon station. Since this region is fully covered by the forward chambers we do not expect any trigger loss.

Clearly a tuning procedure of the BTI model could be performed in any of the situations considered in order to maximize the BTI efficiency. We have chosen to setup the device only once at B = 0T in order to understand the extension of the range in which the BTI performance was not significantly affected from drift line deformations due to magnetic field.

5. Conclusions

The beam test of the fixed angle prototype version of the BTI, realized in FPGA, was quite satisfactory. Once all the effects of the design limitations are considered, the performance of the device fully agrees with expectations.

The collected drift time measurements were used to perform the simulation of the full scale device with real data. The results confirm the validity of the design choices and are completely coherent with all the previously performed computations.

The performance degradation in the magnetic field expected in the CMS detector should be relatively small, although further work is needed for a more precise evaluation of the related effects.

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Fig. Captions

Fig. 1 - Exemplification of the bunch crossing identification and the track candidate measurement.

Fig. 2 - BTI geometric layout showing the channels allocation and important parameters.

Fig. 3 - Shift register of a couple of wires in the FPGA prototype. The grey area shows the acceptance. The input position in the upper shift register is programmable as a function of the track inclination.

Fig. 4 - Trigger rate of the BTI at the expected step (see text) as a function of the difference in phase between the FPGA prototype clock and the experiment trigger.

Fig. 5 - Trigger rate of the BTI model versus the synchronization time. The setup time is set using two time parameters (the shift register length and a programmable delay).

Fig. 6 - Example of the distribution of the BTI triggers, before LTS application in the model, around the expected step: the HTRGs are almost only at the expected step, while the LTRGs are dispersed.

Fig. 7 - Comparison of the measured efficiency versus the track inclination for the FPGA prototype and the BTI model with and without LTS.

Fig. 8 - Definition of magnetic field components.

Fig. 9 - Efficiency of the BTI software model as a function of B_w for several track inclinations. The lines are drawn just to guide the eye.

B_V(T)	0.0	0.5	1.5
B_n(T)	0.0	0.0	0.0
B_W(T)	0.0	0.0	0.0
Efficiency	0.943	0.936	0.887

B_V(T)	0.0	0.0	0.0
B_n(T)	0.0	0.5	1.0
B_W(T)	0.0	0.0	0.0
Efficiency	0.943	0.946	0.483

B_V(T)	0.0	0.0	0.0
B_n(T)	0.5	0.49	0.47
B_W(T)	0.0	0.11	0.18
Efficiency	0.946	0.922	0.939

B_V(T)	0.0	0.11	0.18
B_n(T)	0.5	0.49	0.47
B_W(T)	0.0	0.0	0.0
Efficiency	0.946	0.935	0.955

B_V(T)	0.0	0.0	0.0
B_n(T)	1.0	0.98	0.93
B_W(T)	0.0	0.21	0.36
Efficiency	0.482	0.442	0.402

B_V(T)	0.0	0.21	0.36
B_n(T)	1.0	0.98	0.93
B_W(T)	0.0	0.0	0.0
Efficiency	0.482	0.420	0.483

Table 1 - Efficiency of BTI model in several magnetic field configurations.

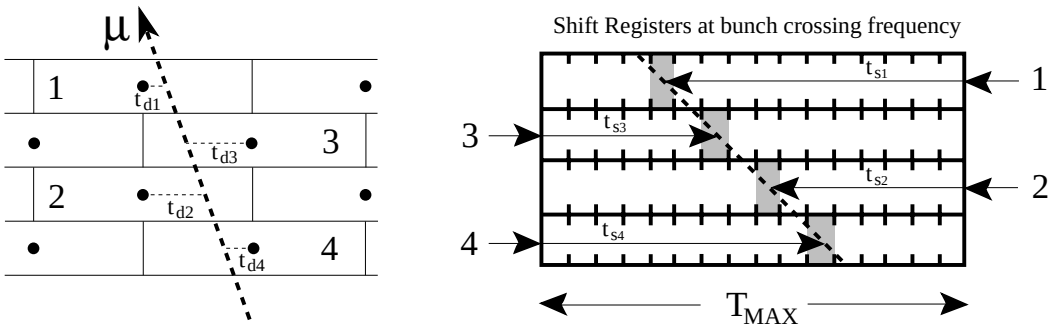
μ
1
2
3
4
t_{d1}
t_{d2}
t_{d3}
t_{d4}
Shift Registers at bunch crossing frequency
t_{s1}
t_{s2}
t_{s3}
t_{s4}
T_{MAX}

Fig. 1

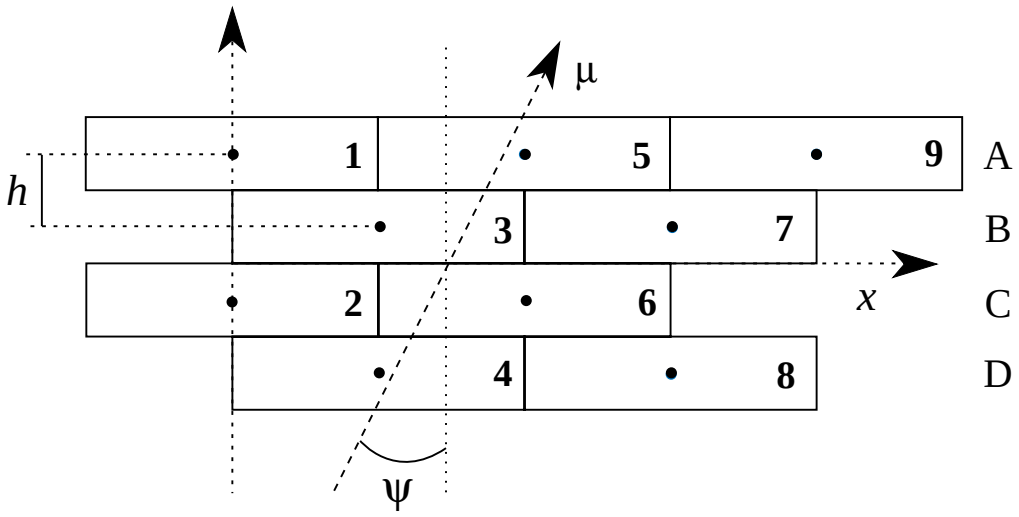
μ
h
1
5
9
A
3
7
B
2
6
x
C
4
8
D
ψ

Fig. 2

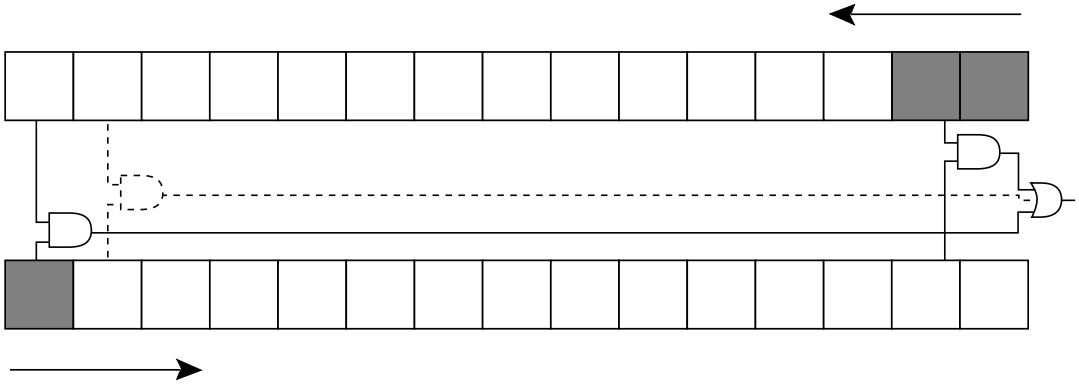

Fig. 3

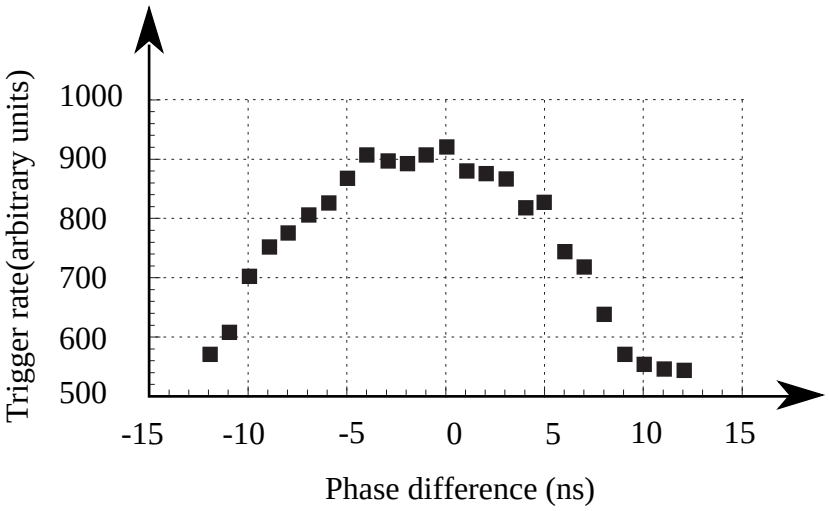
Trigger rate(arbitrary units)
1000
900
800
700
600
500
-15
-10
-5
0
5
10
15
Phase difference (ns)

Fig. 4

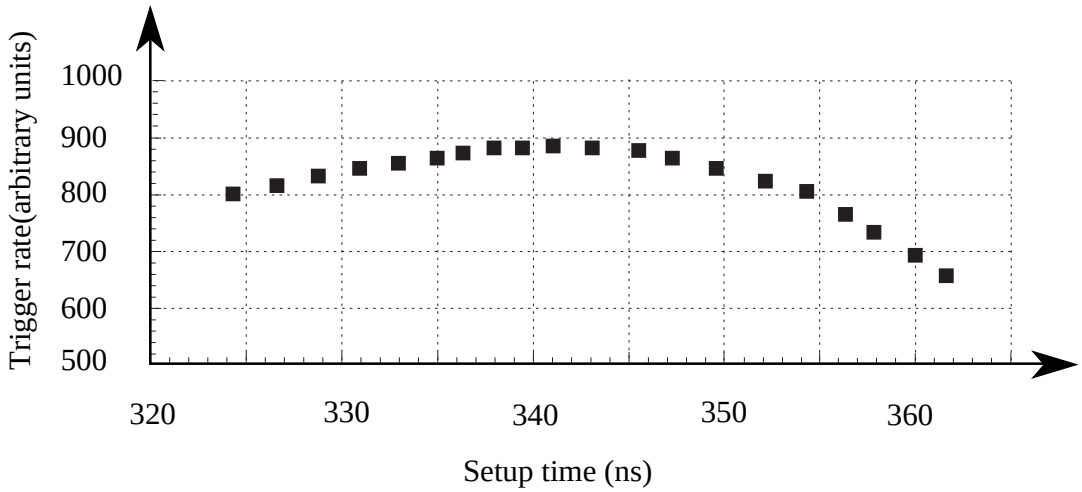
Trigger rate(arbitrary units)
1000
900
800
700
600
500
320
330
340
350
360
Setup time (ns)

Fig. 5

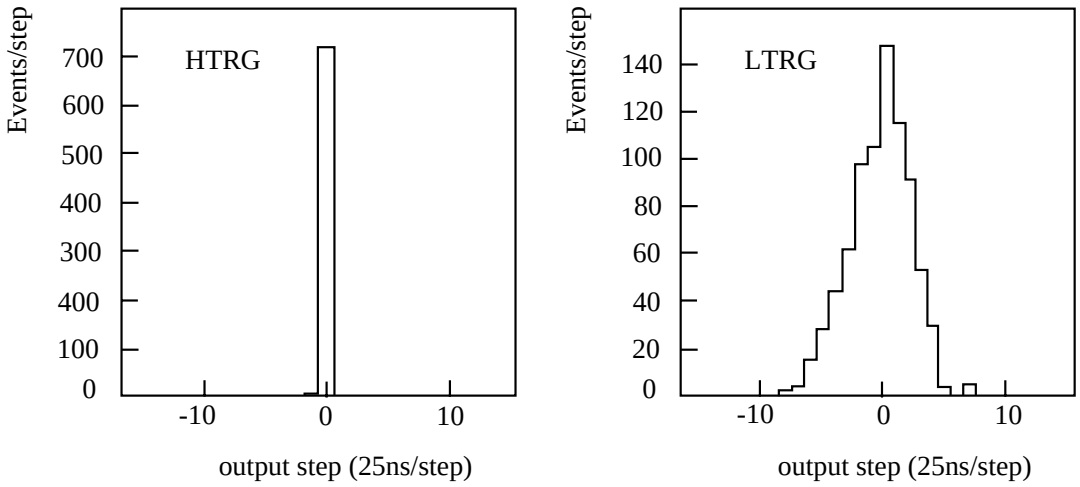
Events/step
HTRG
700
600
500
400
300
400
100
0
-10
0
10
output step (25ns/step)
Events/step
LTRG
140
120
100
80
60
40
20
0
-10
0
10
output step (25ns/step)

Fig. 6

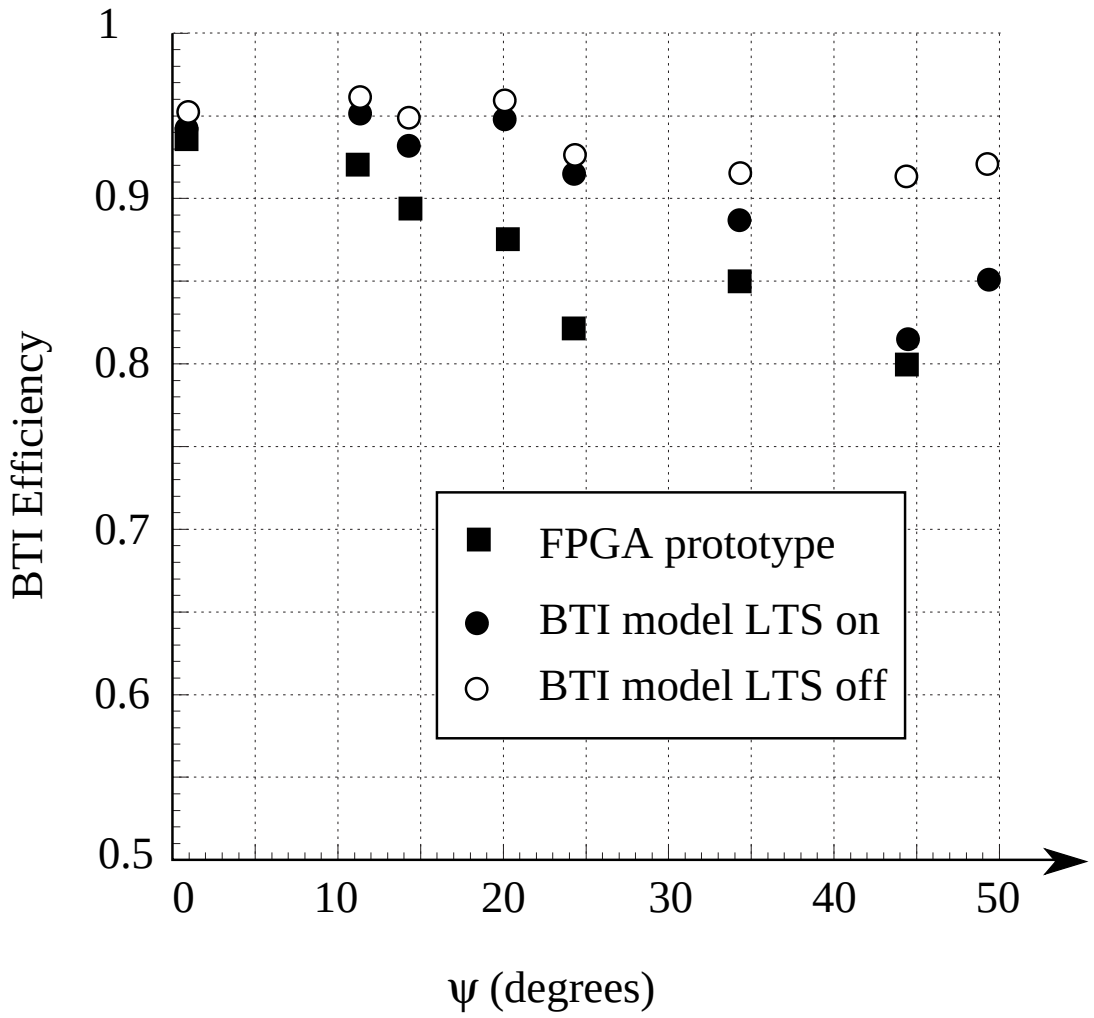
1
0.9
0.8
0.7
0.6
0.5
BTI Efficiency
0
10
20
30
40
50
ψ (degrees)
FPGA prototype
BTI model LTS on
BTI model LTS off

Fig. 7

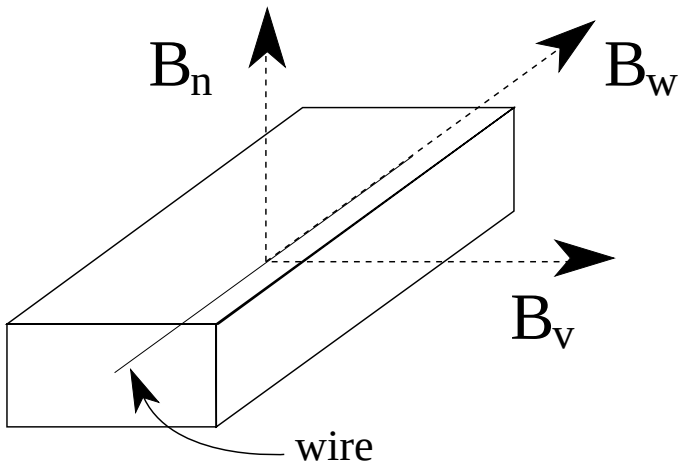
B_n
B_w
B_v
wire

Fig. 8

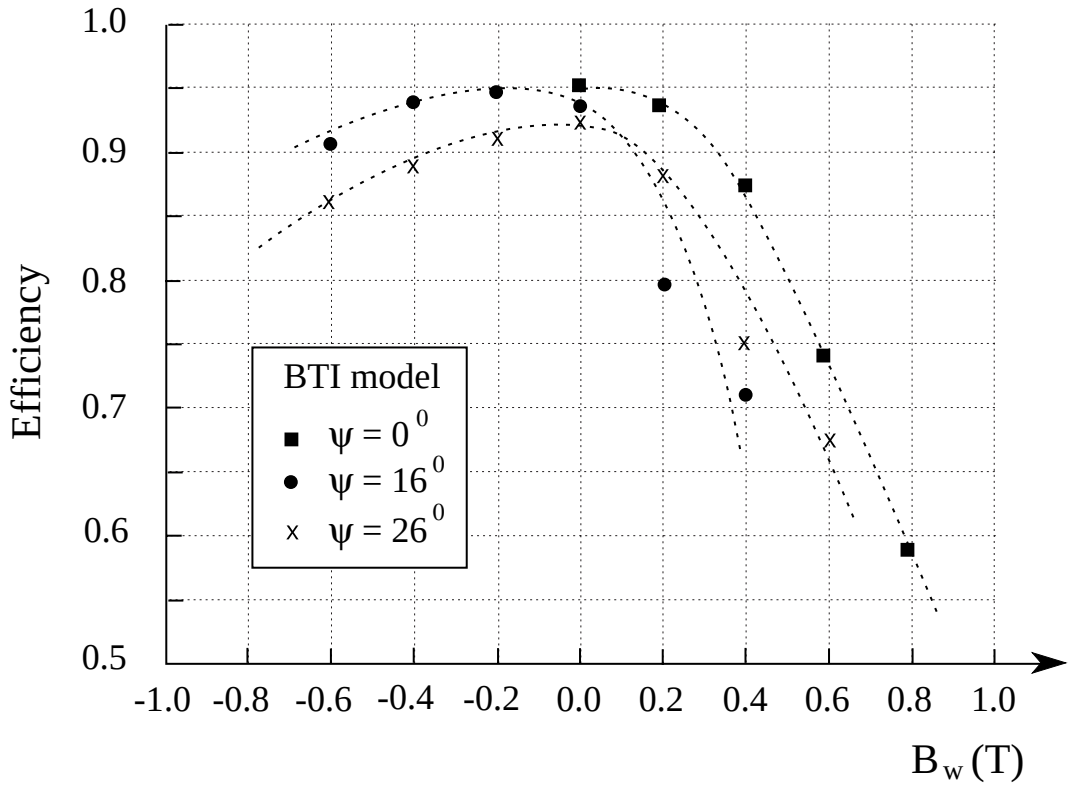
1.0
0.9
0.8
0.7
0.6
0.5
Efficiency
BTI model
ψ = 0 0
ψ = 16 0
ψ = 26 0
-1.0 -0.8 -0.6 -0.4 -0.2 0.0 0.2 0.4 0.6 0.8 1.0
B w (T)

Fig. 9